CS4297A

Preliminary Product Data Sheet

FEATURES

- **AC '97 2.1 Compatible**
- **Industry Leading Mixed Signal Technology**
- **20-bit Stereo Digital-to-Analog Converter and 18-bit Stereo Analog to Digital Converter**
- **Four Analog Line-level Stereo Inputs for Connection from LINE IN, CD, VIDEO, and AUX**
- **Two Analog Line-level Mono Inputs for Modem Subsystem and Internal PC Beeper**
- **Mono Microphone Input Switchable from Two External Sources**
- **High Quality Pseudo Differential CD Input**
- **Dual Stereo Line-level Outputs**
- **Extensive Power Management Support**
- **Meets or Exceeds Microsoft's® PC 98 and PC 99 Audio Performance Requirements**
- **CrystalClear 3D Stereo Enhancement**
- **S/PDIF Digital Audio Output**

ORDERING INFO

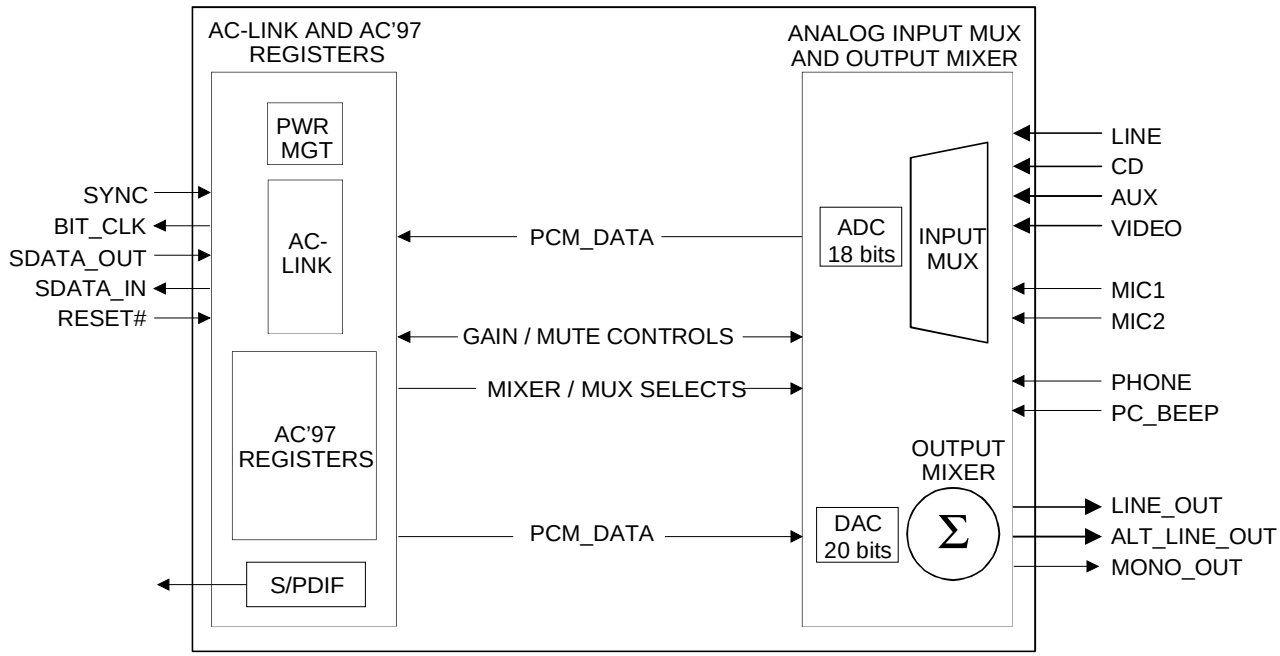
CS4297A-KQ, 48-pin TQFP, 9x9x1 mm
CS4297A-JQ, 48-pin TQFP, 9x9x1 mm

CrystalClear™ SoundFusion™ Audio Codec '97

DESCRIPTION

The CS4297A is an AC '97 2.1 compatible stereo audio codec designed for PC multimedia systems. Using the industry leading CrystalClear delta-sigma and mixed signal technology, the CS4297A paves the way for PC 98 and PC 99-compliant desktop, portable, and entertainment PCs, where high-quality audio is required.

The CS4297A, when coupled with a PCI audio accelerator or core logic supporting the AC '97 interface, implements a cost effective, superior quality, audio solution. The CS4297A surpasses audio quality standards such as PC 98, PC 99, and AC '97 2.1.



Preliminary Product Information | This document contains information for a new product. Cirrus Logic reserves the right to modify this product without notice.

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1.0 CHARACTERISTICS AND SPECIFICATIONS

ANALOG CHARACTERISTICS

(Standard test conditions unless otherwise noted: $T_{ambient}$ = 25° C, AVdd = 5.0 V ±5%, DVdd = 3.3 V ±5%; 1 kHz Input Sine wave; Sample Frequency, Fs = 48 kHz; Z_{AL}=10 kΩ/ 680 pF load, C_{DL} = 18 pF load (Note 1); Measurement bandwidth is 20 Hz - 20 kHz, 18-bit linear coding for ADC functions, 20-bit linear coding for DAC functions; Mixer registers set for unity gain.

Parameter (Note 2)	Symbol	Path (Note 3)	CS4297A-KQ			CS4297A-JQ			Unit
			Min	Typ	Max	Min	Typ	Max	
Full Scale Input Voltage									
Line Inputs		A-D	0.91	1.00	-	0.91	1.00	-	V_{RMS}
Mic Inputs (20dB = 0)		A-D	0.91	1.00	-	0.91	1.00	-	V_{RMS}
Mic Inputs (20dB = 1)		A-D	0.091	0.10	-	0.091	0.10	-	V_{RMS}
Full Scale Output Voltage									
Line,Alternate Line, and Mono Outputs		D-A	0.91	1.0	1.13	0.91	1.0	1.13	V_{RMS}
Frequency Response (Note 4)	FR								
Analog Ac = ± 0.5 dB		A-A	20	-	20,000	20	-	20,000	Hz
DAC Ac = ± 0.5 dB		D-A	20	-	20,000	20	-	20,000	Hz
ADC Ac = ± 0.5 dB		A-D	20	-	20,000	20	-	20,000	Hz
Dynamic Range									
Stereo Analog inputs to LINE_OUT	DR	A-A	90	95	-	-	90	-	dB FS A
Mono Analog inputs to LINE_OUT		A-A	85	90	-	-	85	-	dB FS A
DAC Dynamic Range		D-A	85	90	-	-	87	-	dB FS A
ADC Dynamic Range		A-D	85	90	-	-	85	-	dB FS A
DAC SNR (-20 dB FS input w/ CCIR-RMS filter on output)	SNR	D-A	-	70	-	-	-	-	dB
Total Harmonic Distortion + Noise (-3 dB FS input signal):									
Line/Alternate Line Output	THD+N	A-A	-	-90	-80	-	-	-74	dB FS
DAC		D-A	-	-87	-80	-	-	-74	dB FS
ADC (all inputs except phone/mic)		A-D	-	-84	-80	-	-	-74	dB FS
ADC (phone/mic)		A-D	-	-85	-74	-	-	-74	dB FS
Power Supply Rejection Ratio (1 kHz, 0.5 V_{RMS} w/ 5 V DC offset)(Note 4)			40	60	-	-	40	-	dB
Interchannel Isolation			70	87	-	-	87	-	dB
Spurious Tone (Note 4)			-	-100	-	-	-100	-	dB FS
Input Impedance (Note 4)			10	-	-	10	-	-	kΩ
External Load Impedance			10	-	-	10	-	-	kΩ
Output Impedance (Note 4)			-	730	-	-	730	-	Ω
Input Capacitance (Note 4)			-	5	-	-	5	-	pF
Vrefout			2.0	2.3	2.5	2.0	2.3	2.5	V

Notes:
1. Z_{AL} refers to the analog output pin loading and C_{DL} refers to the digital output pin loading.
2. Parameter definitions are given in the *Parameter and Term Definitions* section.
3. Path refers to the signal path used to generate this data. These paths are defined in the *Parameter and Term Definitions* section.
4. This specification is guaranteed by silicon characterization, it is not production tested.

MIXER CHARACTERISTICS (for CS4297A-KQ only)

Parameter	Min	Typ	Max	Unit
Mixer Gain Range Span				
Line In, Aux, CD, Video, Mic1 Mic2, Phone, PC Beep, Alternate Line	-	46.5	-	dB
Mono Out	-	46.5	-	dB
Line Out	-	94.5	-	dB
Step Size				
All volume controls except PC Beep	-	1.5	-	dB
PC Beep	-	3.0	-	dB

ABSOLUTE MAXIMUM RATINGS (AVss1 = AVss2 = DVss1 = DVss2 = 0 V)

Parameter		Min	Typ	Max	Unit
Power Supplies	+3.3 V Digital	-0.3	-	6.0	V
	+5 V Digital	-0.3	-	6.0	V
	Analog	-0.3	-	6.0	V
Total Power Dissipation	(Supplies, Inputs, Outputs)	-	-	TBD	mW
Input Current per Pin	(Except Supply Pins)	-10	-	10	mA
Output Current per Pin	(Except Supply Pins)	-15	-	15	mA
Analog Input voltage		-0.3	-	AVdd+ 0.3	V
Digital Input voltage		-0.3	-	DVdd + 0.3	V
Ambient Temperature	(Power Applied)	-55	-	110	°C
Storage Temperature		-65	-	150	°C

RECOMMENDED OPERATING CONDITIONS (AVss1 = AVss2 = DVss1 = DVss2 = 0 V)

Parameter		Symbol	Min	Typ	Max	Unit
Power Supplies	+3.3 V Digital	DVdd1, DVdd2	3.135	3.3	3.465	V
	+5 V Digital	DVdd1, DVdd2	4.75	5	5.25	V
	Analog	AVdd1, AVdd2	4.75	5	5.25	V
Operating Ambient Temperature			0	-	70	°C

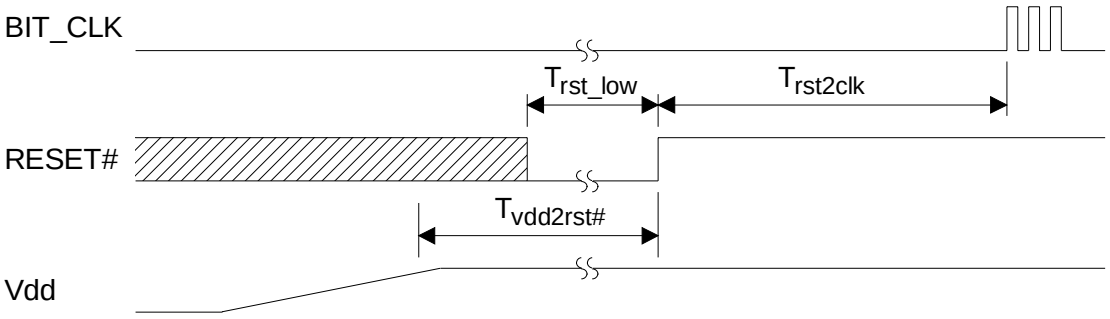
DIGITAL CHARACTERISTICS (AVss = DVss = 0 V (See *Grounding and Layout* section))

Parameter	Symbol	Min	Typ	Max	Unit
Low level input voltage	V_{il}	-	-	0.35 x DVdd	V
High level input voltage	V_{ih}	0.65 x DVdd	-	-	V
High level output voltage	V_{oh}	0.90 x DVdd	0.99 x DVdd	-	V
Low level output voltage	V_{ol}	-	0.03	0.10 x DVdd	V
Input Leakage Current (AC-link inputs)		-10	-	10	µA
Output Leakage Current (Tri-stated AC-link outputs)		-10	-	10	µA
Output buffer drive current (Note 4)		-	TBD		µA

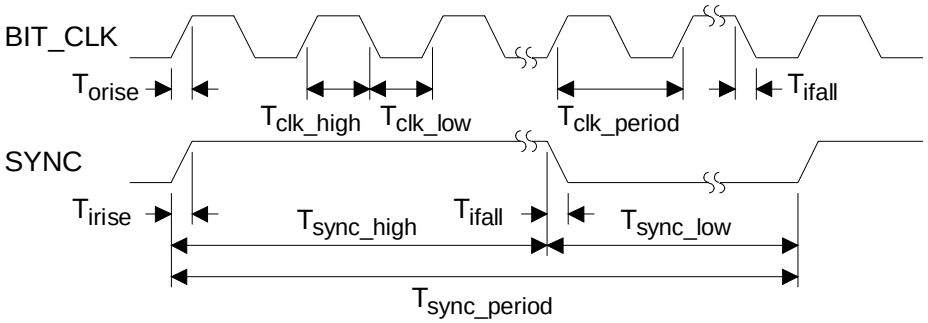
SERIAL PORT TIMING

Standard test conditions unless otherwise noted: $T_{ambient}$ = 25° C, AVdd = 5.0 V, DVdd = 3.3 V; C_L = 55 pF load.

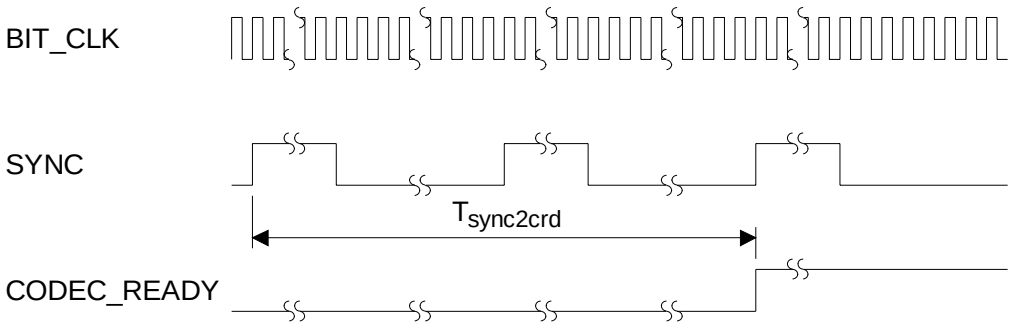
Parameter	Symbol	Min	Typ	Max	Unit
RESET Timing					
RESET# active low pulse width	T_{rst_low}	1.0	-	-	µs
RESET# inactive to BIT_CLK start-up delay	$T_{rst2clk}$	-	TBD	-	ms
1st SYNC active to CODEC READY set	$T_{sync2crd}$	-	41.6	-	µs
Vdd stable to Reset inactive	$T_{vdd2rst\#}$		TBD		
Clocks					
BIT_CLK frequency	F_{clk}	-	12.288	-	MHz
BIT_CLK period	T_{clk_period}	-	81.4	-	ns
BIT_CLK output jitter (depends on XTAL_IN source)		-	-	750	ps
BIT_CLK high pulse width	T_{clk_high}	36	40.7	45	ns
BIT_CLK low pulse width	T_{clk_low}	36	40.7	45	ns
SYNC frequency	F_{sync}	-	48	-	kHz
SYNC period	T_{sync_period}	-	20.8	-	µs
SYNC high pulse width	T_{sync_high}	-	1.3	-	µs
SYNC low pulse width	T_{sync_low}	-	19.5	-	µs
Data Setup and Hold					
Output Propagation delay from rising edge of BIT_CLK	T_{prop}	-	6	8	ns
Output hold from falling edge of BIT_CLK	T_{ohold}	5	-	-	ns
Input setup time from falling edge of BIT_CLK	T_{isetup}	10	-	-	ns
Input hold time from falling edge of BIT_CLK	T_{ihold}	0	-	-	ns
Input Signal rise time	T_{irise}	2	-	6	ns
Input Signal fall time	T_{ifall}	2	-	6	ns
Output Signal rise time (Note 4)	T_{orise}	2	4	6	ns
Output Signal fall time (Note 4)	T_{ofall}	2	4	6	ns
Misc. Timing Parameters					
End of Slot 2 to BIT_CLK, SDATA_IN low (PR4)	T_{s2_pdown}	-	.34	1.0	µs
SYNC pulse width (PR4) Warm Reset	T_{sync_pr4}	1.0	-	-	µs
SYNC inactive (PR4) to BIT_CLK start-up delay	$T_{sync2clk}$	162.8	244	-	ns
Setup to trailing edge of RESET# (ATE test mode) (Note 4)	$T_{setup2rst}$	15	-	-	ns
Rising edge of RESET# to Hi-Z delay (Note 4)	T_{off}	-	-	25	ns



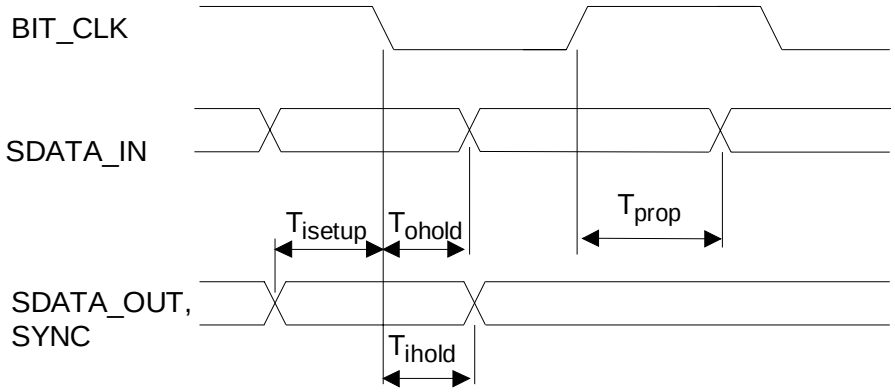
Power Up Timing



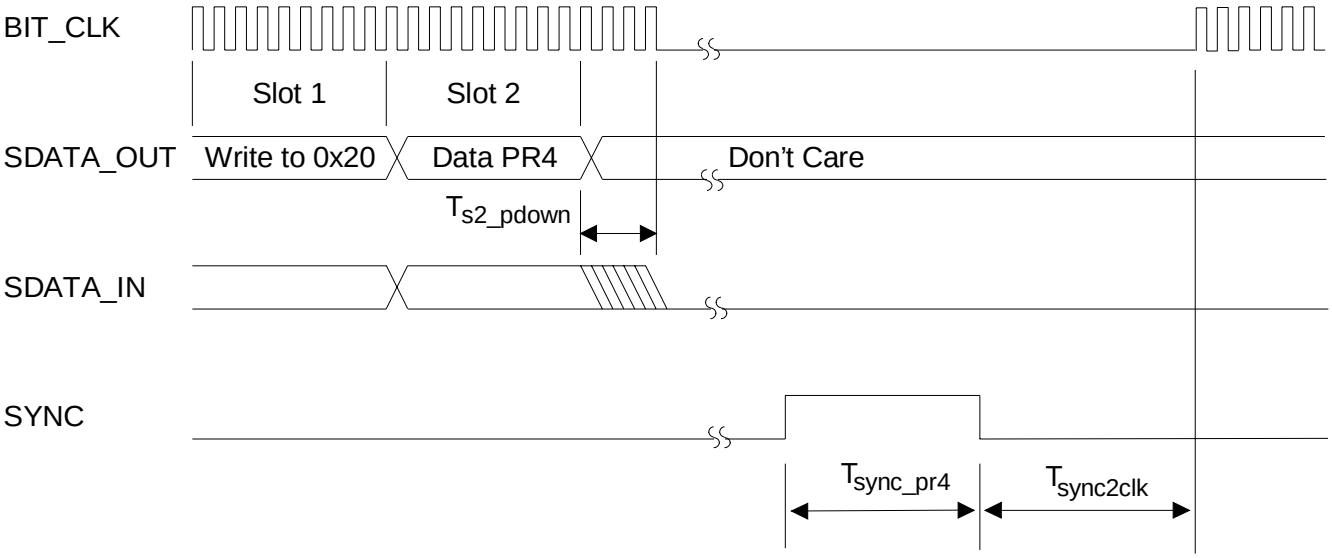
Clocks



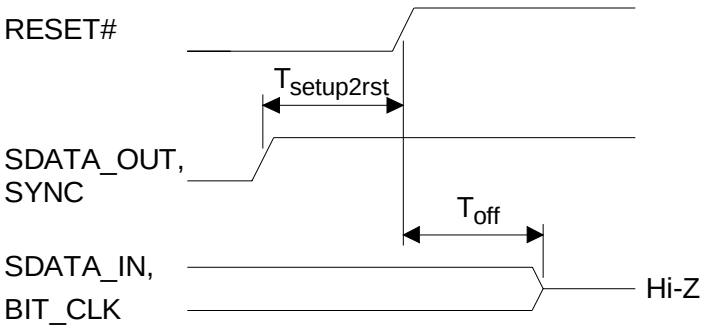
Codec Ready from Startup or Fault Condition



Data Setup and Hold



PR4 Powerdown and Warm Reset



Test Mode

2.0 GENERAL DESCRIPTION

The CS4297A is a mixed-signal serial Codec compliant to the *Audio Codec '97 Specification*, revision 2.1 [1]. It is designed to be paired with a digital interface, referred to as the Controller, which is typically located on the PCI bus or integrated within the system chip set. The Controller is responsible for all communications between the CS4297A and the remainder of the system. The Codec contains two distinct functional sections: Digital and Analog. The Digital section includes the AC-link registers, power management support, and AC-link serial port interface logic. The analog section includes the analog input multiplexer (mux), stereo output mixer, mono output mixer, stereo ADCs, stereo DACs, and their associated volume controls.

2.1 AC-Link

All communication with the Codec is established with a 5-wire digital interface to the Controller chip as shown in Figure 1. All clocking for the serial communication is synchronous to the BIT_CLK signal. BIT_CLK is generated by the primary Codec and is used to slave the Controller and any secondary Codecs, if applicable. An AC-link audio frame is a sequence of 256 serial bits organized into 13 groups referred to as 'slots'. One frame consists of one 16-bit slot and twelve 20-bit slots. During each audio frame, data is passed bi-directionally between the Codec and the Controller. The input frame is driven from the Codec on the SDATA_IN line. The output frame is driven from the Controller SDATA_OUT line. Both input and output frames contain the same number of bits and are organized with the same 'slot' configuration. The input and output frame have differing functions for each slot. The Controller synchronizes the beginning of a frame with the SYNC signal. In Figure 2 the position of each bit location within the frame is noted. The first bit position in a new serial data frame is F0 and the last bit position in the serial data frame is F255. When SYNC goes active (high) and is sampled active by the CS4297A (on the falling edge of BIT_CLK), both devices are synchronized to a new serial data frame. The data on the SDATA_OUT pin at this clock edge is the final bit of the previous frame's serial data. On the next rising edge of BIT_CLK, the first bit of Slot 0 is driven by the Controller on the SDATA_OUT pin. The CS4297A latches in this data, as the first bit of the frame, on the next falling edge of the BIT_CLK clock signal. The Controller is also responsible for issuing reset via the RESET# signal. After being reset, the Codec is responsible for flagging the Controller that it is ready for operation after synchronizing its internal functions. The AC-link signals may be referenced to either 5 Volts or 3.3 Volts. The CS4297A must use the same digital supply voltage as the Controller chip.

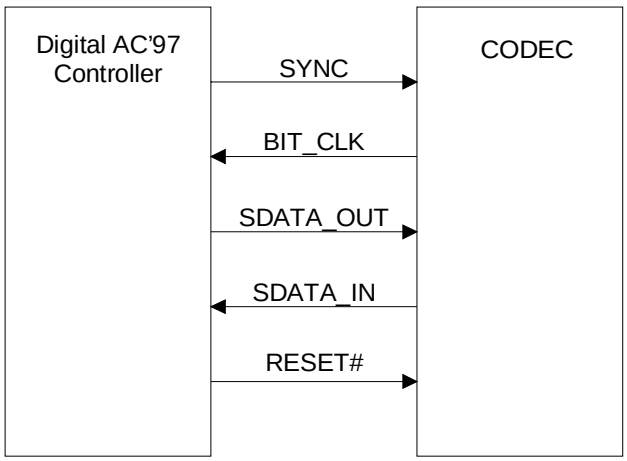


Figure 1. AC-link Connections

2.2 Control registers

All read accesses to the Codec are generated by requesting a register address (index number) in slot 1 of a SDATA_OUT frame. The following SDATA_IN frame will contain the register content in its

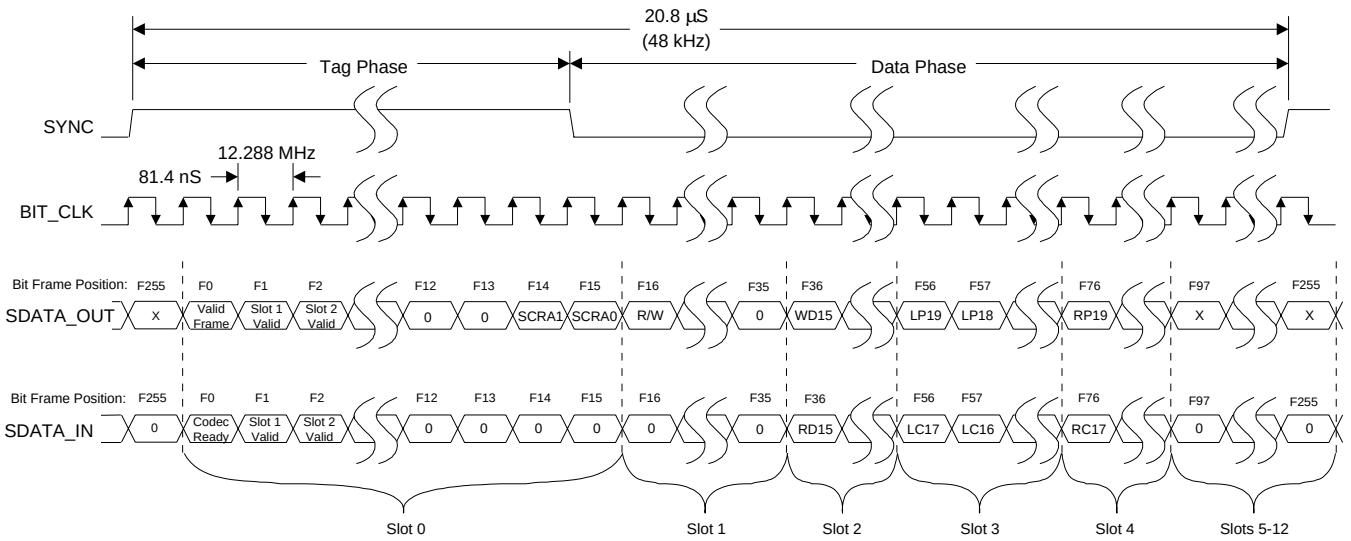


Figure 2. AC-link Input and Output Framing

slot 2. The write operation is identical with the index in slot 1 and the write data in slot 2. The *AC '97 Frame Definition* section details the function of each input and output frame. Individual register descriptions are found in the *Register Interface* section.

2.3 Output Mixer

There are two output mixers on the CS4297A as illustrated in Figure 3. The stereo output mixer sums together the analog inputs to the CS4297A according to the settings in the volume control registers. The mono output mixer generates a monophonic sum of the left and right channels from the stereo input mixer. However, the mono output mixer does not include the PC_BEEP and PHONE signals which are included in the stereo output mix. The stereo output mix is sent to the LINE_OUT and ALT_LINE_OUT output pins of the CS4297A. The mono output mix is sent to the MONO_OUT output pin on the CS4297A.

2.4 Input Mux

The input multiplexer controls which analog input is sent to the ADCs. The output of the input mux is converted to stereo 18-bit digital PCM data and sent to the Controller chip the AC-link SDATA_IN signal.

2.5 Volume Control

The Codec's volume control registers control analog input level to the input mixer, the master volume level, and the alternate volume level. All analog volume controls, except PC_BEEP, implement controlled volume steps at nominally 1.5 dB per step. PC_BEEP uses 3 dB steps. The analog inputs allow a mixing range of +12 dB of signal gain to -34.5 dB of signal attenuation. The analog output volume controls allow from 0 dB to -94.5 dB of attenuation for LINE_OUT and -46.5 dB for ALT_LINE_OUT and MONO_OUT. The PC_BEEP input volume control allows from 0 dB to -45 dB of attenuation.

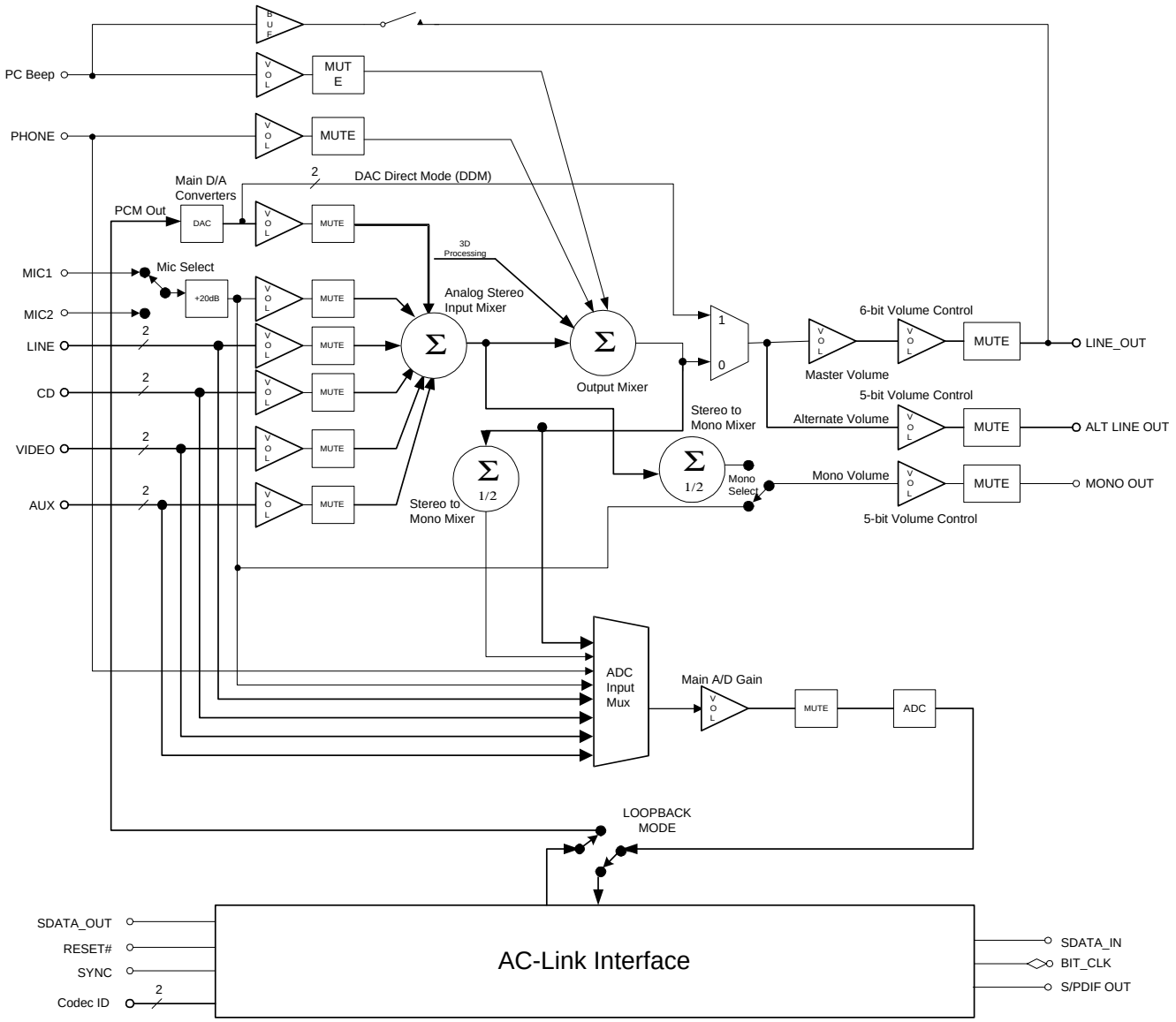


Figure 3. Mixer Diagram

3.0 AC '97 FRAME DEFINITION

The AC Link is a bi-directional serial port with thirteen time-division multiplexed slots in each direction. The first slot is 16 bits long and termed the tag slot. Bits in the tag slot determine if the Codec is ready and indicate which, if any, other slots contain valid data. Slots 1 through 12 are 20-bits long and can contain audio data. Slot 11 and Slot 12 are not utilized on the CS4297A. The serial data line is defined from the Controller's perspective, NOT from the Audio Codec's perspective.

3.1 AC-Link Serial Data Output Frame

In the serial data output frame, data is passed on the SDATA_OUT pin TO the CS4297A FROM the Controller. Figure 2 illustrates the serial port timing.

Serial Data Output Slot Tags (Slot 0)

Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Valid Frame	Slot 1 Valid	Slot 2 Valid	Slot 3 Valid	Slot 4 Valid	Slot 5 Valid	Slot 6 Valid	Slot 7 Valid	Slot 8 Valid	Slot 9 Valid	Slot 10 Valid				SCRA 1	SCRA 0

Valid Frame — Determines if any of the following slots contain either valid playback data for the Codec's DACs or data for read/write operation. When set, at least one of the other AC-link slots contain valid data. If this bit is clear, the remainder of the frame is ignored.

Slot [1:2] Valid — Indicates valid slot data when accessing the register set of the primary Codec (SCRA[1:0] = 00). For a read operation, Slot 1 Valid is set when *Register Address* (Slot 1) contains valid data. For a write operation, Slot 1 Valid and Slot 2 Valid are set indicating *Register Address* (Slot 1) and *Register Write Data* (Slot 2) contain valid data. The register address and write data must be valid within the same frame. SCRA[1:0] must be cleared when accessing the primary Codec. The physical address of a Codec is determined by the ID[1:0]# input pins which are reflected in the *Extended Audio ID* (Index 28h) register.

Slot [3:10] Valid — If a Slot Valid bit is set, the named slot contains valid audio data. If the bit is clear, the slot will be ignored. The Codec supports alternate slot mapping as defined in the AC '97 2.1 specification [1]. For more information, see the *Slot Map* (Index 5Eh) register.

SCRA[1:0] — Secondary Codec Register Access. Unlike the primary Codec, SCRA[1:0] indicate valid slot data when accessing the register set of a secondary Codec. The value set in SCRA[1:0] (01,10,11) determines which of the three possible secondary Codecs is accessed. For a read operation, the SCRA[1:0] bits are set when *Register Address* (Slot 1) contains valid data. For a write operation, SCRA[1:0] bits are set when *Register Address* (Slot 1) and *Register Write Data* (Slot 2) contain valid data. The write operation requires the register address and the write data to be valid within the same frame. SCRA[1:0] must be cleared when accessing the primary Codec. They must also be cleared during the idle period where no register read or write is pending. The physical address of a Codec is determined by the ID[1:0]# input pins which are reflected in the *Extended Audio ID* (Index 28h) register. The SCRA[1:0] bits are listed as the ID[1:0] bits in Slot 0 in the AC '97 specification.

Register Address (Slot 1)

Bit 19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/$\overline{W}$	RI6	RI5	RI4	RI3	RI2	RI1	RI0												

R/$\overline{W}$ — Read/$\overline{\text{Write}}$. Determines if a read (R/$\overline{W}$ = 1) or write (R/$\overline{W}$ = 0) operation is requested. For a read operation, the following Input Frame will return the register index in the *Read-Back Address Port* (Slot 1) and the contents of the register in the *Read-Back Data Port* (Slot 2). A write operation does not return any valid data in the following frame. If the R/$\overline{W}$ bit = 0, data must be valid in both the *Register Address* (Slot 1) and the *Register Write Data* (Slot 2) during a frame when Slot [1:2] Valid or SCRA[1:0] are set.

RI[6:0] Register index/address. Registers can only be accessed on word boundaries; RI0 must be set to 0. RI[6:0] must contain valid data during a frame when the Slot 1 Valid or SCRA[1:0] are set.

Register Write Data (Slot 2)

Bit 19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WD15	WD14	WD13	WD12	WD11	WD10	WD9	WD8	WD7	WD6	WD5	WD4	WD3	WD2	WD1	WD0				

WD[15:0] Codec register data for write operations. For read operations, this data is ignored. If R/$\overline{W}$ = 0, data must be valid in both the *Register Address* (Slot 1) and the *Register Write Data* (Slot 2) during a frame when the Slot [1:2] Valid = 11 or either SCRA[1:0] bit is set. Splitting the register address and the write data across multiple frames is not permitted.

Playback Data (Slots 3-10)

Bit 19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PD19	PD18	PD17	PD16	PD15	PD14	PD13	PD12	PD11	PD10	PD9	PD8	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0

PD[19:0] 20-bit PCM playback (2's compliment) data for the left and right DACs and/or the S/PDIF transmitter. Any PCM data from the Controller less than 20 bits should be left justified in the slot and zero-padded. Table 7 on page 23 lists the definition of each respective slot. The mapping of a given slot to a DAC is determined by the state of the ID[1:0] bits found in the *Extended Audio ID* (Index 28h) register and by the SM[1:0] and AMAP bits found in the *Slot Map* (Index 5Eh) register.

3.2 AC-Link Audio Input Frame

In the serial data input frame, data is passed on the SDATA_IN pin FROM the CS4297A to the AC '97 Controller. The data format for the input frame is very similar to the output frame. Figure 2 illustrates the serial port timing.

Serial Data Input Slot Tag Bits (Slot 0)

Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Codec Ready	Slot 1 Valid	Slot 2 Valid	Slot 3 Valid	Slot 4 Valid	Slot 5 Valid	Slot 6 Valid	Slot 7 Valid	Slot 8 Valid	Slot 9 Valid	Slot 10 Valid					

Codec Ready Indicates the readiness of the CS4297A's AC-link and Control and Status registers. Immediately after a Cold Reset this bit will be clear. Once the CS4297A's clocks and voltages are stable, this bit will be set. Until the Codec Ready bit is set, no AC-link transactions should be attempted by the Controller. The Codec Ready bit does not indicate readiness of the DACs, ADCs, Vref, or any other analog function. Those must be checked in the *Powerdown Control/Status* (Index 26h) register by the Controller before any access is made to the mixer registers. Any accesses to the Codec while Codec Ready is clear is ignored.

Slot 1 Valid Tag

Indicates Slot 1 contains a valid read back address.

Slot 2 Valid Tag

Indicates Slot 2 contains valid register read data.

Slot [3:10] Valid Tag

Indicates Slot [3:10] contains valid capture data from the Codec's ADC.

Read-Back Address Port (Slot 1)

Bit 19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RI6	RI5	RI4	RI3	RI2	RI1	RI0												

RI[6:0] Register index. The Read-Back Address Port echoes the AC '97 Register address when a register read has been requested in the previous frame. The Codec will only echo the register index for a read access. Write accesses will not return valid data in Slot 1.

Read-Back Data Port (Slot 2)

Bit 19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RD15	RD14	RD13	RD12	RD11	RD10	RD9	RD8	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0				

RD[15:0] 16-bit register value. The Read-Back Data Port contains the register data requested by the Controller from the previous read request. All read requests will return the read address in the *Read-Back Address Port* (Slot 1) and the register data in the *Read-Back Data Port* (Slot 2) on the following serial data frame.

PCM Capture Data (Slot 3-10)

Bit 19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CD17	CD16	CD15	CD14	CD13	CD12	CD11	CD10	CD9	CD8	CD7	CD6	CD5	CD4	CD3	CD2	CD1	CD0		

CD[17:0] 18-bit PCM (2's compliment) data. The mapping of a given slot to an ADC is determined by the state of the ID[1:0] bits found in the *Extended Audio ID* (Index 28h) register and the SM[1:0] and AMAP bits found in the *Slot Map* (Index 5Eh) register. The definition of each slot can be found in Table 6 on page 23.

The capture data in Slot [3:10] will only be valid when the respective slot valid bit is set in Slot 0.

3.3 AC '97 Reset Modes

Three methods of resetting the CS4297A, as defined in the AC '97 Specification, are supported: *Cold AC '97 Reset*, *Warm AC '97 Reset*, and *AC '97 Register Reset*. A Cold AC '97 Reset is required to restart the AC-link when bit PR5 is set in the *Powerdown Control/Status* (Index 26h) register.

Cold AC '97 Reset

A Cold Reset is performed by asserting RESET# in accordance with the minimum timing specifications in the *Serial Port Timing* section. Once de-asserted, all of the Codec's registers will be reset to their default power-on states and the BIT_CLK clock and SDATA_IN signals will be reactivated. The timing of power-up/reset events is discussed in detail in the *Power Management* section.

Warm AC '97 Reset

The CS4297A may also be reactivated when the AC-link is powered down (refer to the PR4 bit description in the *Power Management* section) by a Warm Reset. A Warm Reset allows the AC-link to be reactivated without losing information in the Codec's registers. Warm Reset is initiated when the SYNC signal is driven high for at least 1 µs and then driven low in the absence of the BIT_CLK clock signal. The BIT_CLK clock will not restart until at least 2 normal BIT_CLK clock periods (± 162.8 ns) after the SYNC signal is de-asserted.

AC '97 Register Reset

The third reset mode provides a register reset to the CS4297A. This is available only when the CS4297A's AC-link is active and the Codec Ready bit is set. The Register Reset forces all registers to be reset to their default, power-up values. A Register Reset occurs when any value is written to the *Reset* (Index 00h) register.

3.4 AC-Link Protocol Violation - Loss of SYNC

The CS4297A is designed to handle SYNC protocol violations. The following are situations where the SYNC protocol has been violated:

- The SYNC signal is not sampled high for exactly 16 BIT_CLK clock cycles at the start of an audio frame.
- The SYNC signal is not sampled high on the 256th BIT_CLK clock period after the previous SYNC assertion.
- The SYNC signal goes active high before the 256th BIT_CLK clock period after the previous SYNC assertion.

Upon loss of synchronization with the Controller, the Codec will mute all analog outputs and clear the Codec Ready bit in the serial data input frame until two valid frames are detected. During this detection period, the Codec will ignore all register reads and writes and will discontinue the transmission of PCM capture data.

4.0 REGISTER INTERFACE

Reg Num	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
00h	Reset		SE4	SE3	SE2	SE1	SE0	ID9	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	1990h
02h	Master Volume	Mute		ML5	ML4	ML3	ML2	ML1	ML0			MR5	MR4	MR3	MR2	MR1	MR0	8000h
04h	Alternate Line Out Volume	Mute			ML4	ML3	ML2	ML1	ML0				MR4	MR3	MR2	MR1	MR0	8000h
06h	Master Volume Mono	Mute											MM4	MM3	MM2	MM1	MM0	8000h
0Ah	PC_BEEP Volume	Mute											PV3	PV2	PV1	PV0		0000h
0Ch	Phone Volume	Mute											GN4	GN3	GN2	GN1	GN0	8008h
0Eh	Mic Volume	Mute									20dB		GN4	GN3	GN2	GN1	GN0	8008h
10h	Line In Volume	Mute			GL4	GL3	GL2	GL1	GL0				GR4	GR3	GR2	GR1	GR0	8808h
12h	CD Volume	Mute			GL4	GL3	GL2	GL1	GL0				GR4	GR3	GR2	GR1	GR0	8808h
14h	Video Volume	Mute			GL4	GL3	GL2	GL1	GL0				GR4	GR3	GR2	GR1	GR0	8808h
16h	Aux Volume	Mute			GL4	GL3	GL2	GL1	GL0				GR4	GR3	GR2	GR1	GR0	8808h
18h	PCM Out Vol	Mute			GL4	GL3	GL2	GL1	GL0				GR4	GR3	GR2	GR1	GR0	8808h
1Ah	Record Select						SL2	SL1	SL0						SR2	SR1	SR0	0000h
1Ch	Record Gain	Mute				GL3	GL2	GL1	GL0					GR3	GR2	GR1	GR0	8000h
20h	General Purpose			3D				MIX	MS	LPBK								0000h
22h	3D Control													S3	S2	S1	S0	0000h
26h	Powerdown Ctrl/Stat	EAPD	PR6	PR5	PR4	PR3	PR2	PR1	PR0					REF	ANL	DAC	ADC	000Fh
28h	Extended Audio ID	ID1	ID0					AMAP									VRA	0200h
2Ch	PCM Front DAC Rate	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h
32h	PCM Left/Right ADC Rate	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h
Cirrus Defined Registers:																		
5E	Slot Map Register								DDM	AMEN		SM1	SM0					0080h
68	S/PDIF Enable	SPEN	V		Fg	L	CC6	CC5	CC4	CC3	CC2	CC1	CC0	Pre	Copy	#Audio		0000h
7Ch	Vendor ID1(CR)	F7	F6	F5	F4	F3	F4	F1	F0	S7	S6	S5	S4	S3	S2	S1	S0	4352h
7Eh	Vendor ID2(Y-)	T7	T6	T5	T4	T3	T2	T1	T0		CID2	CID1	CID0		RID2	RID1	RID0	5911h

Table 1. Mixer Registers

Reset (Index 00h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	SE4	SE3	SE2	SE1	SE0	0	ID8	ID7	0	0	ID4	0	0	0	0

SE[4:0] 3D Stereo Enhancement Technique.
00110 - Crystal 3D Stereo Enhancement.

ID8 set 18-bit ADC resolution.

ID7 set 20-bit DAC resolution.

ID4 set Headphone out support. (Alternate Line Output)

Read-only data 1990h

Any write to this register causes a Register Reset of the Codec's registers forcing all registers to their default state. Reads return configuration information about the Codec.

Master Volume (Index 02h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Mute		ML5	ML4	ML3	ML2	ML1	ML0			MR5	MR4	MR3	MR2	MR1	MR0

Mute Master mute for the LINE_OUT_L and the LINE_OUT_R output signals.

ML[5:0] Master Volume control for LINE_OUT_L pin. Least significant bit represents -1.5 dB with 00000 = 0 dB. The total range is 0 dB to -94.5 dB.

MR[5:0] Master Volume control for LINE_OUT_R pin. Least significant bit represents -1.5 dB with 00000 = 0 dB. The total range is 0 dB to -94.5 dB.

Default 8000h, corresponding to 0 dB attenuation and mute on.

Alternate Volume (Index 04h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Mute		ML5	ML4	ML3	ML2	ML1	ML0			MR5	MR4	MR3	MR2	MR1	MR0

Mute Master mute for the ALT_LINE_OUT_L and the ALT_LINE_OUT_R output signals.

ML[4:0] Master Volume control for ALT_LINE_OUT_L pin. Least significant bit represents -1.5 dB with 00000 = 0 dB. The total range is 0 dB to -46.5 dB.

ML5 Setting ML5 sets the left channel attenuation to -46.5 dB by forcing ML[4:0] to a 1 state. ML[5:0] will read back 01111 when ML5 has been set. See Table 2.

MR[4:0] Master Volume control for ALT_LINE_OUT_R pin. Least significant bit represents -1.5 dB with 00000 = 0 dB. The total range is 0 dB to -46.5 dB.

MR5 Setting MR5 sets the right channel attenuation to -46.5 dB by forcing MR[4:0] to a 1 state. MR[5:0] will read back 011111 when MR5 has been set. See Table 2.

Default 8000h, corresponding to 0 dB attenuation and mute on.

ML[5:0]/MR[5:0]/MM[5:0] Write	**ML[5:0]/MR[5:0]/MM[5:0 Read**	**Gain Level**
000000	000000	0 dB
000001	000001	-1.5 dB
…	…	...
011111	011111	-46.5 dB
...	...	...
1xxxxx	011111	-46.5 dB

Table 2. Alternate Line-Out and Master Mono Attenuation

Master Mono Volume (Index 06h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Mute										MM5	MM4	MM3	MM2	MM1	MM0

Mute — When set, mutes the MONO_OUT signal.

MM[4:0] — Master Mono Attenuation. Least significant bit represents -1.5 dB with 00000 = 0 dB. The total range is 0 dB to -46.5 dB.

MM5 — Setting MM5 sets the master mono attenuation to -46.5 dB by forcing MM[4:0] to a 1 state. MM[5:0] will read back 011111 when MM5 has been set. See Table 2.

Default — 8000h, corresponding to 0 dB attenuation and Mute set.

PC_BEEP Volume (Index 0Ah)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Mute											PV3	PV2	PV1	PV0	

Mute — When set, mutes the PC_BEEP signal.

PV[3:0] — Volume Control for PC_BEEP pin. Least significant bit represents -3 dB with 0000 = 0 dB. The total range is 0 dB to -45 dB.

Default — 0000h, Unmuted, with 0 dB attenuation after the CS4297A is removed from the reset state.

Phone Volume (Index 0Ch)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Mute											GN4	GN3	GN2	GN1	GN0

Mute — When set mutes the Phone signal.

GN[4:0] — Phone Volume Control. Least significant bit represents 1.5 dB with 01000 = 0 dB. The total range is 12 dB to -34.5 dB.

Default — 8008h, 0 dB attenuation and Mute set.

Microphone Volume (Index 0Eh)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Mute									20dB		GN4	GN3	GN2	GN1	GN0

Mute — When set, mutes MIC1/MIC2 signal.

GN[4:0] — MIC1/MIC2 Volume Control. Least significant bit represents 1.5 dB with 01000 = 0 dB. The total range is 12 dB to -34.5 dB.

20dB — Enables 20 dB microphone gain block.

Default — 8008h, 0 dB attenuation and Mute set.

This register controls the gain level of the Microphone input source to the Input Mixer. It also controls the +20 dB gain block which connects to the input volume control and to the Input Record Mux. The selection of MIC1 or MIC2 input pins is controlled by the MS bit in the *General Purpose* (Index 20h) register. The gain mapping for this register is shown in Table 3.

GN4 - GN0	Gain Level	Mic Gain with 20dB = 1
00000	+12.0 dB	+32.0 dB
00001	+10.5 dB	30.5 dB
…	…	...
00111	+1.5 dB	21.5 dB
01000	0.0 dB	20.0 dB
01001	-1.5 dB	18.5 dB
…	…	...
11111	-34.5 dB	-14.5 dB

Table 3. Analog Mixer Input Gain Values

Stereo Analog Mixer Input Gain (Index's 10h - 18h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Mute			GL4	GL3	GL2	GL1	GL0				GR4	GR3	GR2	GR1	GR0

Mute When set mutes the respective input. Setting this bit mutes both right and left inputs.

GL[4:0] Left Volume Control. Least significant bit represents 1.5 dB with 01000 = 0 dB. The total range is 12 dB to -34.5 dB. See Table 3.

GR[4:0] Right Volume Control. Least significant bit represents 1.5 dB with 01000 = 0 dB. The total range is 12 dB to -34.5 dB. See Table 3.

Default 8808h, 0 dB gain with Mute enabled.

These registers control the gain levels of the analog input sources to the Input Mixer. The analog inputs associated with registers 10h-18h are found in Table 4.

Register Index	Function
10h	Line IN Volume
12h	CD Volume
14h	Video Volume
16h	Aux Volume
18h	PCM Out Volume

Table 4. Stereo Volume Register Index

Input Mux Select (Index 1Ah)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
					SL2	SL1	SL0						SR2	SR1	SR0

SL[2:0] Left Channel ADC input source select.

SR[2:0] Right Channel ADC input source select.

Default 0000h, MIC inputs selected for both channels.

When capturing PCM data, this register controls the input MUX for the ADCs. Table 5 below lists the possible values for each input.

Sx2 - Sx0	Record Source
0	MIC
1	CD Input
2	Video Input
3	AUX Input
4	Line Input
5	Stereo Mix
6	Mono Mix
7	Phone Input

Table 5. Input Mux Selection

Record Gain (Index 1Ch)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Mute				GL3	GL2	GL1	GL0					GR3	GR2	GR1	GR0

Mute When set, mutes the input to the ADCs.

GL[3:0] Left ADC gain. Least significant bit represents +1.5 dB with 0000 = 0 dB. The total range is 0 dB to +22.5 dB.

GR[3:0] Right ADC gain. Least significant bit represents +1.5 dB with 0000 = 0 dB. The total range is 0 dB to +22.5 dB.

Default 8000h, 0 dB gain with Mute on.

General Purpose (Index 20h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
		3D				MIX	MS	LPBK							

MIX Mono Output Path. When clear, the Mono Mix out (a mix of the 5 analog stereo sources plus PCM_OUT) is selected for MONO_OUT. When set, the MIC path is sent to Mono Out.

MS Microphone Select. Determines which of the two MIC inputs are passed to the mixer. When set, MIC2 input is selected; when clear MIC1 is selected.

LPBK Loopback. If set, enables ADC/DAC Loopback Mode.

3D 3D Enable. If set, enables the CrystalClear 3D stereo enhancement.

Default 0000h.

3D Control (Index 22h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
												S3	S2	S1	S0

S[3:0] Spacial Enhancement Depth. Spacial Enhancement is enabled by the 3D bit in the *General Purpose* (Index 20h) register.
0000 - No spacial enhancement.
1111 - Full special enhancement.

Default 0000h, no spacial enhancement added.

Powerdown Control/Status (Index 26h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
EAPD	PR6	PR5	PR4	PR3	PR2	PR1	PR0					REF	ANL	DAC	ADC

EAPD — External Amplifier Power Down. The EAPD pin follows this bit. Generally used to power-down external amplifiers.

PR6 — When set, the alternate line-out buffer is powered down.

PR5 — When set, the internal master clock is disabled. The only way to recover from setting this bit is through a cold AC '97 reset (driving the RESET# signal active).

PR4 — When set, the AC link is powered down. The AC link can be restarted through a warm AC '97 reset using the SYNC signal, or a cold AC '97 reset using the RESET# signal (the primary codec only).

PR3 — When set, the analog mixer and voltage reference are powered down. When clearing this bit, the ANL, ADC, and DAC bits should be checked before writing any mixer registers.

PR2 — When set, the analog mixer is powered down (the voltage reference is still active). When clearing this bit, the ANL bit should be checked before writing any mixer registers.

PR1 — When set, the DACs are powered down. When clearing this bit, the DAC bit should be checked before sending any data to the DACs.

PR0 — When set, the ADCs and the ADC input muxes are powered down. When clearing this bit, no valid data will be sent down the AC link until the ADC bit goes high.

REF — Voltage Reference Ready Status. When set, indicates the voltage reference is at a nominal level.

ANL — Analog Ready Status. When set, the analog output mixer, input multiplexer, and volume controls are ready. When clear, no volume control registers should be written.

DAC — DAC Ready Status. When set, the DACs are ready to receive data across the AC link. When clear, the DACs will not accept any valid data.

ADC — ADC Ready Status. When set, the ADCs are ready to send data across the AC link. When clear, no data will be sent to the Controller.

Default — 0000h, all blocks are powered on. The lower four bits will eventually change as the Codec finishes an initialization and calibration sequence.

The PR[6:0] and the EAPD bits are power-down control for different sections of the Codec as well as external amplifiers. The REF, ANL, DAC, and ADC bits are status bits which, when set, indicate that a particular section of the Codec is ready. After the Controller receives the Codec Ready bit in Slot 0, these status bits must be checked before writing to any mixer registers.

Extended Audio ID (Index 28h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
ID1	ID0					AMAP									VRA

ID[1:0] — Codec configuration ID. Primary is 00; Secondary is 01,10,or 11. This is a reflection of the ID[1:0]# configuration pins. The state of the ID# pins are determined at power-up and are the inverse of the ID bits in this register.

AMAP — AC Link Mapping. When set, this device supports the AC '97, revision 2.1, AC-link slot to audio DAC mapping. This is a reflection of the AMEN bit in the *Slot Map* (Index 5Eh) register.

VRA — Variable Rate Audio. This bit is clear for the CS4297A indicating variable sample rates are not supported.

Read-only data x200h. Where x is determined by the state of ID[1:0] input pins.

PCM Front DAC Rate (Index 2Ch)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0

SR[15:0] Front DAC Sample Rate.

Read-only value BB80h, indicating 48 kHz sample rate.

PCM LR ADC Rate (Index 32h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0

SR[15:0] Left / Right ADC Sample Rate.

Read-only value BB80h, indicating 48 kHz sample rate.

Slot Map (Index 5Eh)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
							DDM	AMEN		SM1	SM0				

DDM DAC Direct Mode. This bit controls the source to the line and alternate line output drivers. When set, the Left and Right DAC directly drive the line and alternate line outputs by bypassing the audio mixer. When clear, the audio mixer is the source for the line and alternate line outputs.

AMEN Alternate Slot Map Enable. This bit determines if the CS4297A responds to the Codec ID to slot mapping. If clear, the slot mapping will be determined by the state of the SM[1:0] bits. If set, the slot mapping will be determined by the state of the ID[1:0] bits of the *Extended Audio ID* (Index 28h) register.

SM[1:0] Slot Map. Determine which AC-link Slots the ADC and DAC data are transferred through. See Table 6 and Table 7.

Default 0080h

AMEN, SM[1:0] and the ID[1:0] bits of the *Extended Audio ID* (Index 28h) register define the slots assigned for the capture ADCs and the playback DACs. The capture slot assignments are listed in Table 6 and the playback slot assignments are in Table 7.

Slot	Frame definition	ID1	ID0	AMAP*	SM1	SM0	ADC Mapping
3	Left Channel PCM Capture Data	X	X	0	0	0	Left
		0	X	1	X	X	Left
4	Right Channel PCM Capture Data	X	X	0	0	0	Right
		0	X	1	0	0	Right
5	Right Channel PCM Capture Data	X	X	0	0	1	Left
6	Microphone	X	X	0	0	1	Right
		1	1	1	X	X	Left
7	Left Channel PCM Capture Data	X	X	0	1	0	Left
		1	0	1	X	X	Left
8	Right Channel PCM Capture Data	X	X	0	1	0	Right
		1	0	1	X	X	Right
9	Left Channel PCM Capture Data	X	X	0	1	1	Left
		1	1	1	X	X	Right
10	Right Channel PCM Capture Data	X	X	0	1	1	Right
11	Unused						
12							

* AMAP is controlled by AMEN located in *Slot Map* (Index 5Eh) register.

Table 6. Capture Slot Assignments

Slot	Frame definition	ID1	ID0	AMAP*	SM1	SM0	DAC Mapping
3	Left Channel PCM Playback Data	X	X	0	0	0	Left
		0	X	1	X	X	Left
4	Right Channel PCM Playback Data	X	X	0	0	0	Right
		0	X	1	X	X	Right
5	Modem Line 1 PCM Output Data	X	X	0	0	1	Left
6	PCM Center Channel Output Data	X	X	0	0	1	Right
		1	1	1	X	X	Left
7	PCM Left Surround Channel Output Data	X	X	0	1	0	Left
		1	0	1	X	X	Left
8	PCM Right Surround Channel Output Data	X	X	0	1	0	Right
		1	0	1	X	X	Right
9	PCM Low Frequency Effects Output Data	X	X	0	1	1	Left
		1	1	1	X	X	Right
10	Modem Line 1 PCM Output Data	X	X	0	1	1	Right
11	Unused						
12							

* AMAP is controlled by AMEN located in *Slot Map* (Index 5Eh) register.

Table 7. Playback Slot Assignment

S/PDIF Control (Index 68h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
SPEN	V	0	0	L	CC6	CC5	CC4	CC3	CC2	CC1	CC0	Pre	Copy	#Audio	

Please contact Crystal Semiconductor for additional information on the S/PDIF Control Register.

Default 0000h.

Vendor ID1 (Index 7Ch)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
F7	F6	F5	F4	F3	F2	F1	F0	S7	S6	S5	S4	S3	S2	S1	S0

F[7:0] First Character of Vendor ID.
43h - ASCII 'C' character.

S[7:0] Second Character of Vendor ID.
52h - ASCII 'R' character.

Read-only data 4352h.

Vendor ID2 (Index 7Eh)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
T7	T6	T5	T4	T3	T2	T1	T0		PID2	PID1	PID0		RID2	RID1	RID0

T[7:0] Third Character of Vendor ID.
59h - ASCII 'Y' character.

PID[2:0] Part ID.
001 - CS4297A

RID[2:0] Revision.
001 - Revision 'A'.

Read-only data 5911h.

The two Vendor ID registers provide a means to determine the manufacturer of the AC '97 Codec. The first three bytes of the ID registers contain the ASCII code for the first 3 letters of Crystal (CRY). The final byte of the Vendor ID2 register is divided into a Part ID field and a Revision field. Table 8 lists the Part ID's defined to date.

CID2-CID0	Part Name
000	CS4297
001	CS4297A
010	CS4294/CS4298
011	CS4299

Table 8. Reg. 7Eh Defined Part ID's

5.0 POWER MANAGEMENT

The *Powerdown Control/Status* register (Index 26h) controls the power management functions. Seven of these bits (bits 14:8) have defined functions. In effect, all portions of the Codec can be shut down individually and powered back up by a single cold or warm reset sequence. Table 9 shows the mapping of the power control bits to the functions they manage:

PR Bit	Function
PR0	Main ADC's and Input Mux Powerdown
PR1	Main DAC's Powerdown
PR2	Analog Mixer Powerdown (Vref on)
PR3	Analog Mixer Powerdown (Vref off)
PR4	AC-link Powerdown (BIT_CLK off)*
PR5	Internal Clock Disable
PR6	Alternate Line Out Buffer Powerdown

* Applies only to primary Codec

Table 9. Powerdown PR Bit Functions

When, for example, PR0 is set, the main ADC's and the Input Mux are shut down and the ADC bit (bit 0 in the *Powerdown Control/Status* (Index 26h) register) is cleared indicating the ADCs are no longer in a ready state. The same is true for the DACs, the analog mixers, and the reference voltage (Vrefout). When the PR2 or PR3 bit of the mixer is cleared, the mixer section will begin a power-on process, and the corresponding powerdown status bit will be set when the hardware is ready.

Bit PR4, which shuts down the AC-link, causes the primary Codec to turn off the BIT_CLK and drive SDATA_IN low. It also ignores SYNC and SDATA_OUT in their normal capacities. To restore operation to the part from this state, either a cold or a warm reset is required (see *Cold AC '97 Reset* and *Warm AC '97 Reset* sections). A cold reset will restore all mixer registers to their power-on default values. A warm reset will not alter the values of any mixer register (with the exception of clearing the PR4 bit of *Powerdown Control/Status* (Index 26h) register.

The PR5 bit is a global Codec powerdown that forces all internal clocks to shut down. A cold reset is the only way to restore operation to the CS4297A after a global powerdown.

The CS4297A does not automatically mute any input or output when the powerdown bits are set. The software driver controlling the AC '97 device must manage muting the input and output analog signals before putting the part into any power management state.

6.0 ANALOG HARDWARE DESCRIPTION

The analog hardware consist of four line-level stereo inputs, two selectable mono microphone inputs, two mono inputs, a mono output, and dual, independent stereo line outputs. This section describes the analog hardware needed to interface with these pins.

6.1 Line-Level Inputs

The analog inputs consist of four stereo analog inputs and four mono inputs. As shown in Figure 3 on page 11, the input to the ADCs comes from the Input Mux which selects one of the following: Phone (Mono), Aux, Video, CD, Mic1 or Mic2 (Mono), Line, Stereo Output Mix, or the Mono Out-

put Mix (Mono). Unused analog inputs should be connected together and then connected through a capacitor to analog ground or tied to the Vrefout line directly.

The analog input mixer is designed to accommodate five stereo inputs and one mono input. These inputs are: a stereo line-level input (LINE), a mono microphone input (MIC), a stereo CD-ROM input (CD), a stereo auxiliary line-level input (AUX), and the PCM output from the DACs. Each of the stereo inputs has separate volume controls for each channel and one mute control for each left/right pair. The mono microphone input has one mute and one volume control. All analog inputs to the CS4297A, including CD_GND, should be capacitively coupled to the input pins. Since many analog levels can be as large as 2 V_{RMS}, the circuit shown in Figure 4 can be used to attenuate the analog input by 6 dB (to 1 $V_{RMS)}$ which is the maximum voltage allowed for all the stereo line-level inputs.

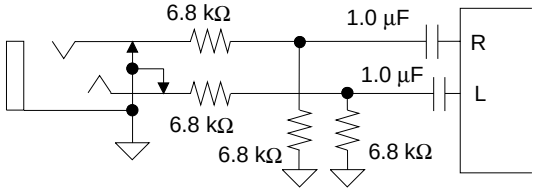


Figure 4. Line Inputs

The CD line-level inputs have an extra pin, CD_GND, which provides a pseudo-differential input for both CD_L and CD_R. This pin takes the common-mode noise out of the CD inputs when connected to the ground coming from the CD analog source. Connecting the CD pins as shown in Figure 5 provides extra attenuation of common mode noise coming from the CDROM drive, thereby producing a higher quality signal. One percent resistors are recommended since the better the resistors match, the better the common-mode attenuation of unwanted signals. If CD is not used, the inputs should be connected through AC capacitors to analog ground or connected to Vrefout.

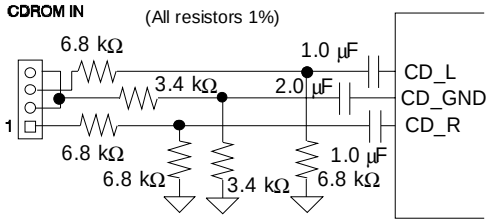


Figure 5. Differential CDROM In

6.2 Microphone Level Inputs

The microphone level inputs, MIC1 and MIC2, include a selectable -34.5 dB to +12 dB gain stage for interfacing to an external microphone. An additional 20 dB gain block is also available. Figure 6 illustrates a single-ended microphone input buffer circuit that will support lower gain dynamic microphones, and phantom-powered microphones that use the right channel (ring) of the jack for power.

6.3 Mono Inputs

The mono input, PC_BEEP, is useful for mixing the output of the "beeper" (timer chip), provided in all PCs, with the rest of the audio signals. When the part is held in reset, the CS4297A passes the PC_BEEP input directly to the line output. This allows the system sounds or "beep" to be available before the AC '97 interface has been activated. This feature is controlled by the BEEP_EN pin. By default, (the BEEP_EN pin unconnected or pulled high) the CS4297A enables the PC_BEEP to line out path while the RESET pin is active. The attenuation control allows 16 levels in -3 dB steps. In addition, a mute control is provided. The attenuator is a single channel block with the resulting signal sent to the output mixer where it is mixed with the left and right outputs. Figure 7 illustrates a typical

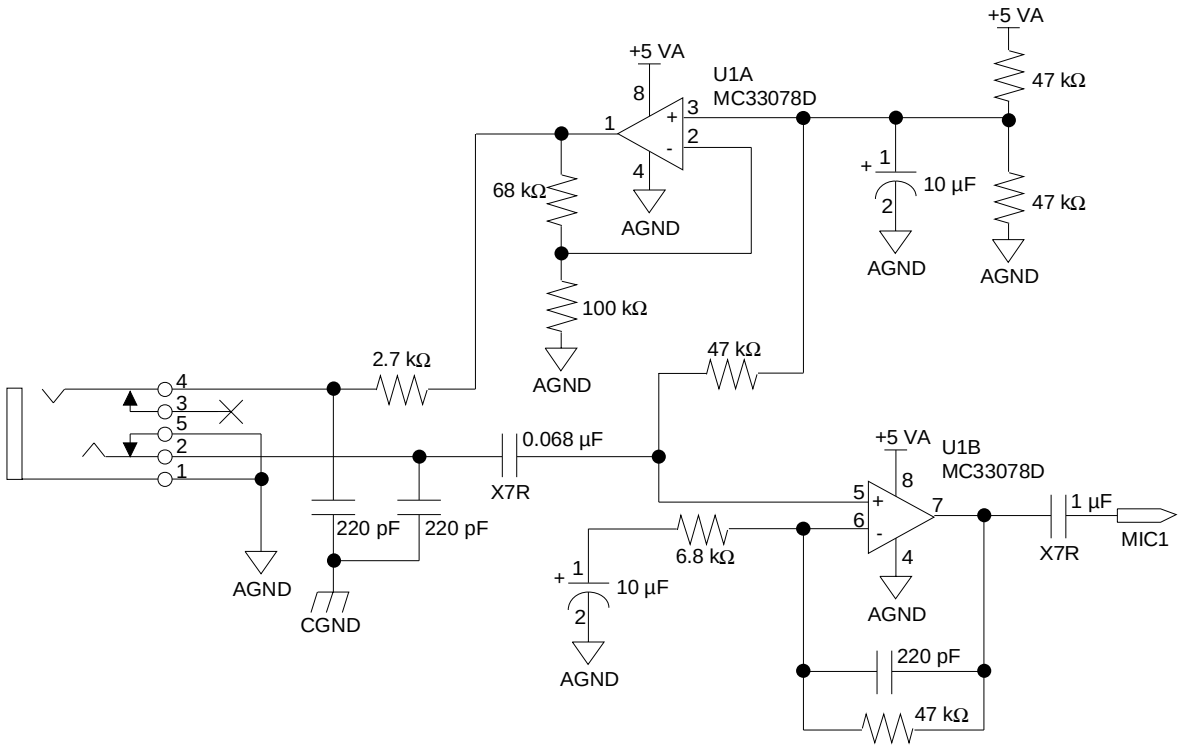


Figure 6. PC '99 Microphone Pre-amplifier

input circuit for the PC_BEEP input. If PC_BEEP is driven from a CMOS gate, the 4.7 kΩ should be tied to analog ground instead of VA+. Although this input is described for a low-quality beeper, the input is of the same high-quality as all other analog inputs and may be used for other purposes.

The mono input, PHONE, can be used to interface to the output of a modem analog front end (AFE) chip so that modem dialing signals and protocol negotiations may be monitored through the audio system. Like all other analog inputs, this pin must be AC coupled and the input signal must be limited to 1 V_{RMS}.

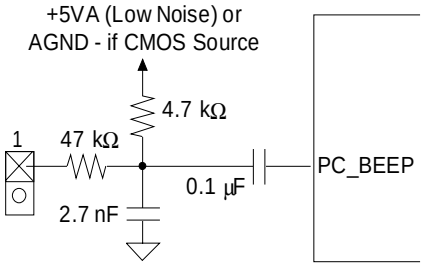


Figure 7. Mono Input

6.4 Line Level Outputs

The analog output section provides a stereo line-level output and an alternate stereo line-level output. LINE_OUT_L, LINE_OUT_R, ALT_LINE_OUT_L, and ALT_LINE_OUT_R outputs should be capacitively coupled to external circuitry.

The mono output, MONO_OUT, can be either a sum of the left and right output channels, attenuated by 6 dB to prevent clipping at full scale, or the selected MIC_IN signal. The mono out channel can drive the PC internal mono speaker using an appropriate buffer circuit The mute control is independent of the line outputs allowing the mono channel to mute the speaker without muting the line outputs.

Each of the 5 analog outputs, if used in the design, require 680 pF to 1000 pF NPO dielectric capacitors between the corresponding pin and analog ground. Each analog output is DC biased up to the Vrefout voltage signal reference which is nominally 2.2 V. This requires that the output either be AC coupled to external circuitry (AC load must be greater than 10 kΩ) or DC coupled to a buffer op-amp biased at the Vrefout voltage (see Figure 8 for the recommended headphone op-amp circuit).

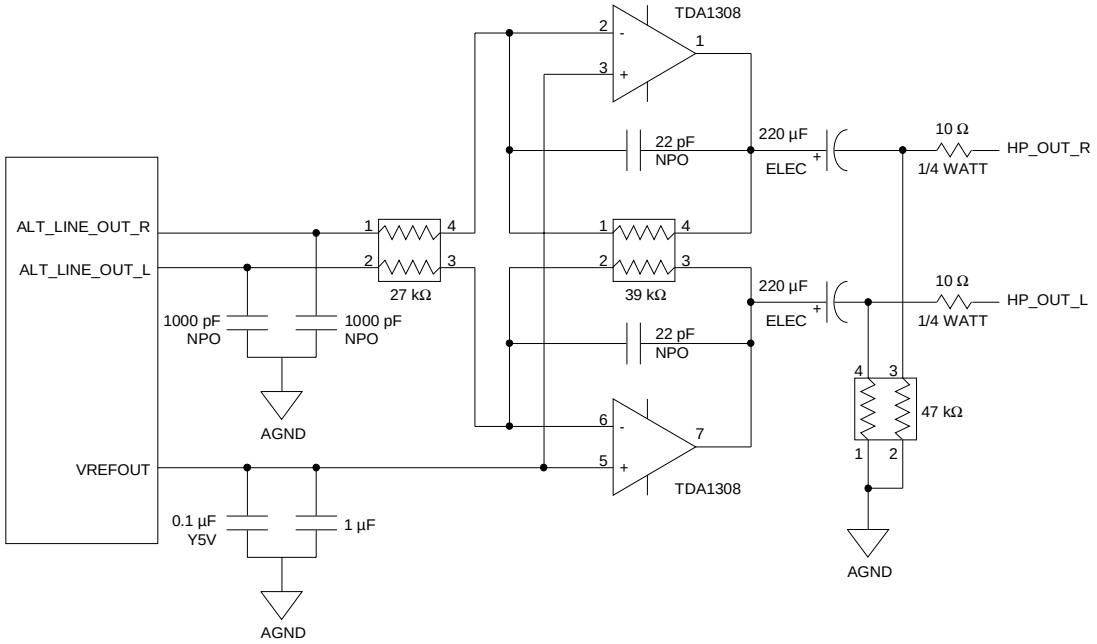


Figure 8. Headphones Driver

6.5 Miscellaneous Analog Signals

The AFLT1 and AFLT2 pins must have a 1000 pF NPO capacitor to analog ground. These capacitors, along with an internal resistor, provide a single-pole low-pass filter at the inputs to the ADCs. By placing these filters at the input to the ADCs, low-pass filters at each analog input pin are not necessary.

The REFFLT pin lowers the noise of the internal voltage reference. A 1 µF (must not be greater than 1 µF) and 0.1 µF capacitor to analog ground should be connected with a short, wide trace to this pin (see Figure 11 in the *Grounding and Layout* section for an example). No other connection should be made, as any coupling onto this pin will degrade the analog performance of the Codec. Likewise, digital signals should be kept away from REFFLT for similar reasons.The Vrefout pin is typically 2.2 V and provides a common mode signal for single-supply external circuits. Vrefout only supports light DC loads and should be buffered if AC loading is needed. For typical use, a 0.1 µF in parallel with a 1 µF capacitor should be connected to Vrefout.

6.6 Consumer IEC-958 Digital Interface (S/PDIF)

The CS4297A supports the industry standard IEC-958 consumer digital interface. Sometimes this interface is referred to as S/PDIF, which refers to an older version of this standard. This output provides an interface, external to the PC, for storing digital audio data or playing digital audio data to digital

speakers. Figure 9 illustrates the circuit necessary for implementation of the IEC-958 optical or consumer interface.

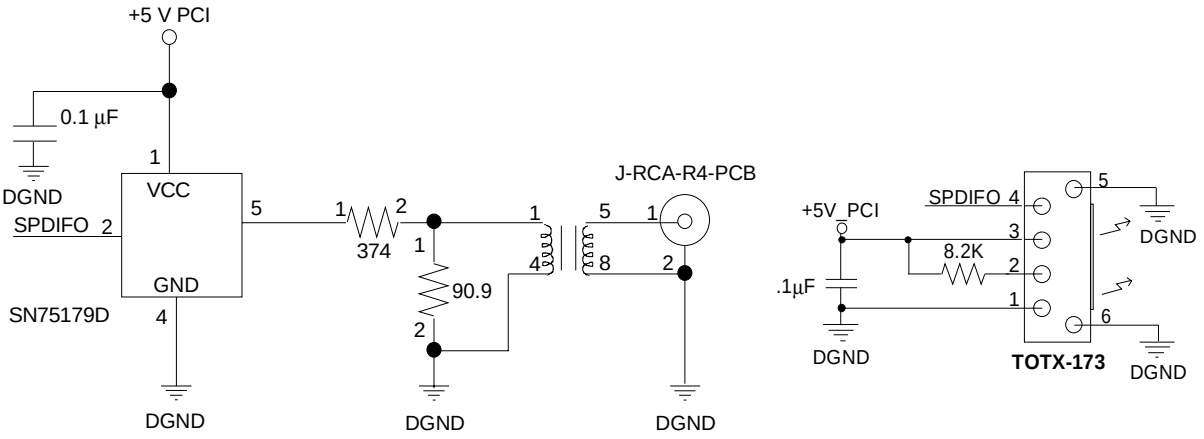


Figure 9. IEC-958 Interface Examples

6.7 Power Supplies

The power supplies providing analog power should be as clean as possible to minimize coupling into the analog section which could degrade analog performance. The pins AVdd1 and AVdd2 supply power to all the analog circuitry on the CS4297A. This 5 Volt analog supply should be generated from a voltage regulator (7805 type) connected to a +12 Volt supply. This helps isolate the analog circuitry from noise typically found on +5 V digital supplies which power many digital circuits in a PC environment. A typical voltage regulator circuit for analog power using an MC78M05CDT is shown in Figure 10. The digital power pins DVdd1 and DVdd2 should be connected to the same digital supply as the Controller's AC-link interface. Since the digital interface on the Codec may operate at either 3.3 V or 5 V, proper connection of these pins will depend on the digital power supply of the Controller.

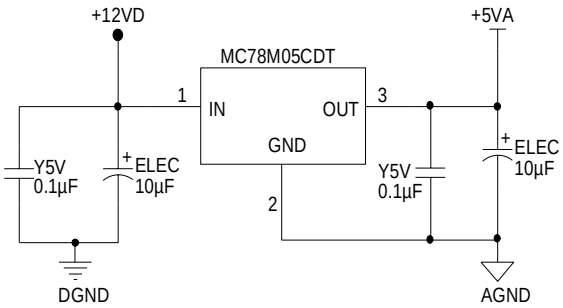


Figure 10. Voltage Regulator

7.0 GROUNDING AND LAYOUT

Figure 11 is the suggested layout for the Codec. The decoupling capacitors should be located physically as close to the pins as possible. Also note the routing of the REFFLT decoupling capacitors and the isolation of that ground strip.

It is strongly recommended that the device be located on a locally separate analog ground plane. This analog ground plane keeps noise from digital ground return currents from modulating the Codec's ground potential and degrading performance. The digital ground pins should be connected to the digital ground plane and kept separate from the analog ground connections of the Codec and any other external analog circuitry.

The common connection point between the two ground planes (required to maintain a common ground voltage potential) should be located near the Codec just under the digital ground connections (vias). The AC-link digital interface connection traces should be routed such that the digital ground plane lies underneath these signals (on the internal ground layer) from the AC '97 Controller continuously to the Codec.

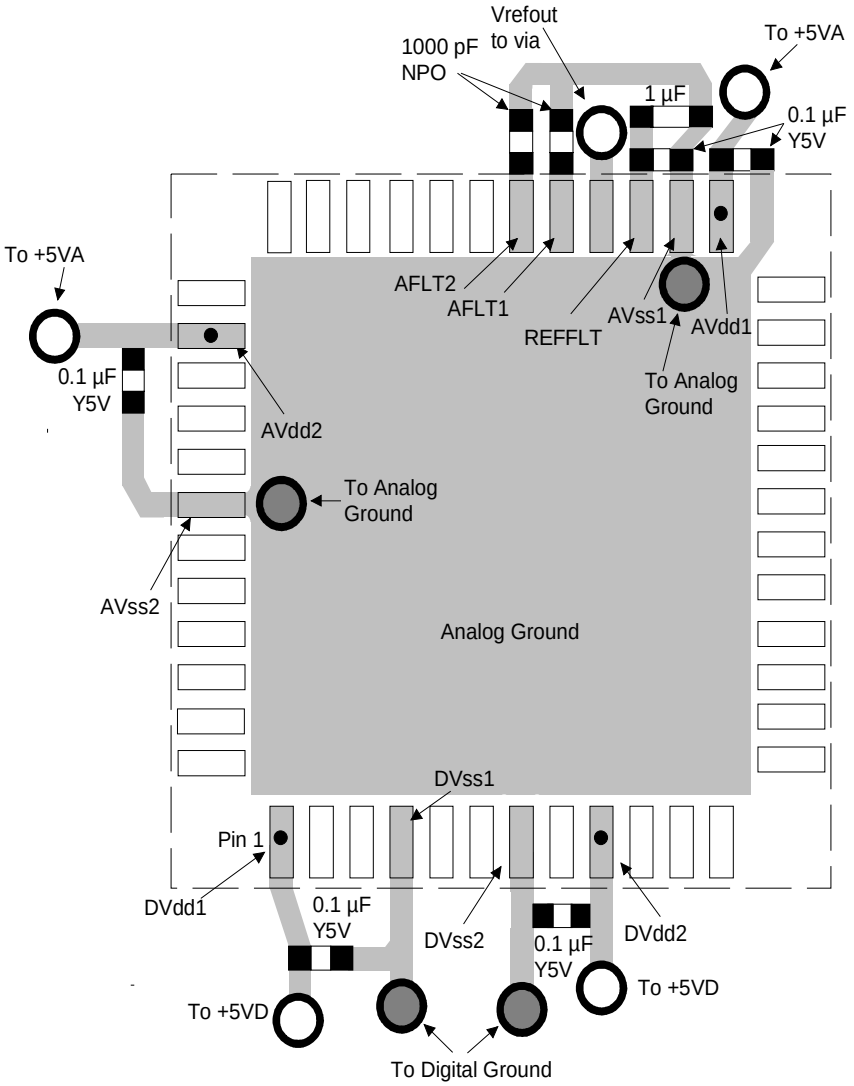
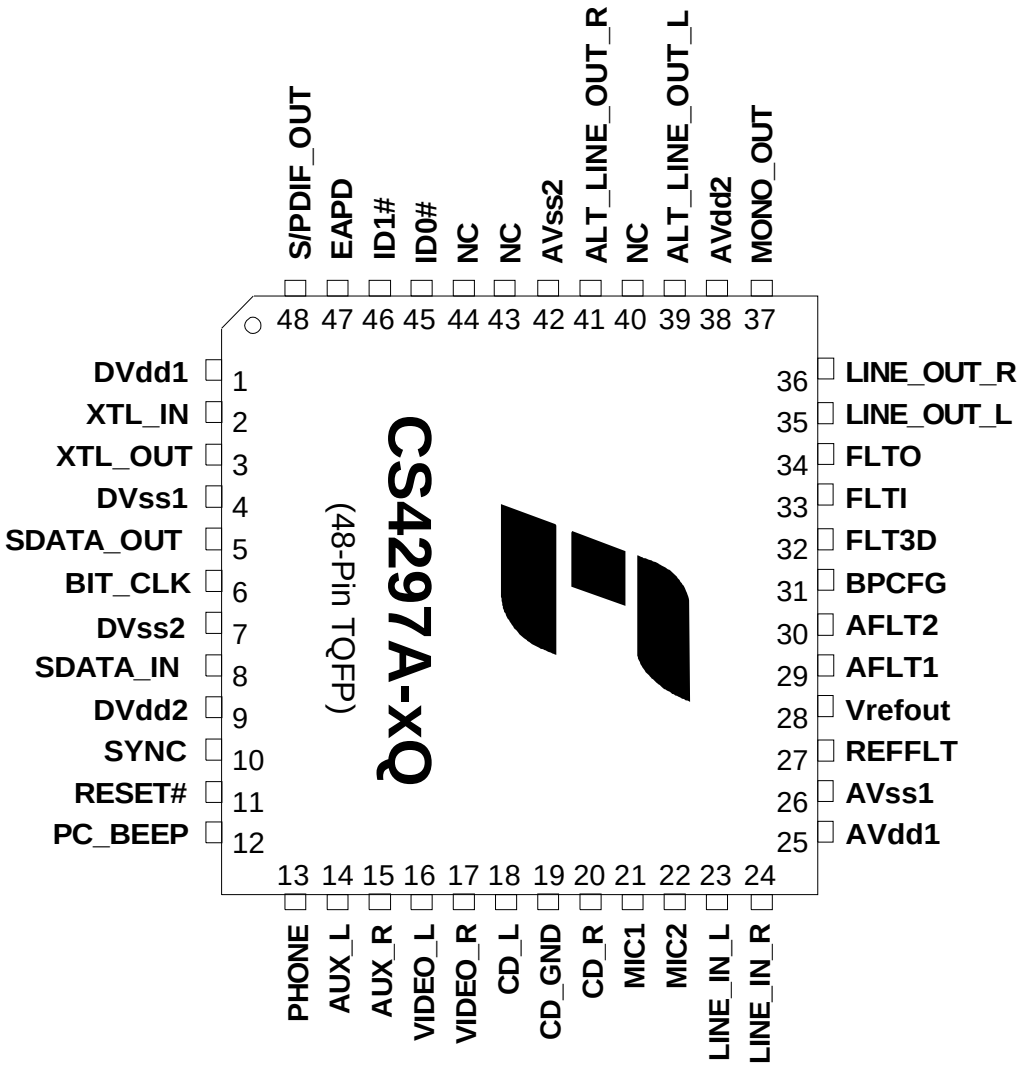


Figure 11. Suggested Layout for the CS4297A

8.0 PIN DESCRIPTIONS



Digital I/O Pins

RESET# - AC '97 Chip Reset, Input

This active low signal is the asynchronous cold reset input to the CS4297A. The CS4297A must be reset before it can enter normal operating mode.

SYNC - AC-Link Serial Port Sync pulse, Input

This signal is the serial port timing signal for the AC-link. Its period is the reciprocal of the sample rate, 48 kHz, and is generated by the AC '97 Controller synchronous to BIT_CLK. SYNC is also an asynchronous input when the Codec is in a warm reset state. A series terminating resistor of 47 Ω should be connected on this signal close to the Controller.

BIT_CLK - AC-Link Serial Port Master Clock, Input/Output

This input/output signal controls the master clock timing for the AC-link. When the Codec is in primary mode, this signal is a 12.288 MHz output clock signal divided down by two from the XTL_IN input clock pin. When the Codec is in secondary mode, this signal is an input which controls the AC-link serial interface and generates all internal clocking. A series terminating resistor of 47 Ω should be connected on this signal close to the primary Codec driving BIT_CLK.

SDATA_OUT - AC-Link Serial Data Input Stream to AC '97, Input

This input signal transmits the control information and digital audio output streams to be sent to the DACs. The data is clocked into the Codec on the falling edge of BIT_CLK. A series terminating resistor of 47 Ω should be connected on this signal close to the Controller.

SDATA_IN - AC-Link Serial Data Output Stream from AC '97, Output

This output signal transmits the status information and digital audio input streams from the ADCs. The data is clocked out of the Codec on the rising edge of BIT_CLK. A series terminating resistor of 47 Ω should be connected on this signal as close to the Codec as possible.

XTL_IN - Crystal Input

When in primary mode, this pin requires either a crystal, with the other pin attached to XTL_OUT, or an external CMOS clock. The crystal frequency must be 24.576 MHz and designed for fundamental mode, parallel resonance operation. When configured as a secondary Codec, all timing is derived from the BIT_CLK input signal; this pin should be left floating.

XTL_OUT - Crystal Output

Used for a crystal placed between this pin and XLT_IN. If an external clock is used on XTL_IN, this pin must be left floating with no traces or components connected to it. When configured as a secondary Codec, this pin should be left floating.

ID1#, ID0# - Codec ID, Inputs

These pins select the Codec ID and mode of operation for the Codec. Their value is sampled and latched on the rising edge of RESET#. These inputs use the digital supply bus for their value and contain internal pull-up resistors to the digital supply bus rail. The pins utilize inverted logic, so a value of '1:1' sets the Codec to primary mode while any other combination sets the Codec to secondary mode. In primary mode, the Codec is always clocked from an external crystal or an external oscillator connected to the XTL_IN and/or XTL_OUT pins with BIT_CLK as an output. When either or both ID's are tied to analog ground, the Codec is in secondary mode and BIT_CLK is always an input.

S/PDIF - IEC-958 Consumer Digital Output, Output

This output provides a digital interface to devices external to the PC. With the appropriate buffer, the output can drive the IEC-958 consumer interface or directly drive an optical transmitter

BPCFG - PC Beep enable, Input

This input controls the PC_BEEP input when the device is held in reset. When unconnected or pulled high through an external pull-up resistor, the PC_BEEP input is enabled. Grounding this input disables the PC_BEEP when reset is active. The pin is pulled high through an internal 100 kΩ resistor.

EAPD - External Amplifier Power Down, Output

This signal is designated as a power down control for audio amplifiers external to the Codec. The output is determined by the EAPD bit and is low by default.

Analog I/O Pins

PC_BEEP - Analog Mono Source, Input

This signal is generally used as an internal PC BEEP connection to the audio subsystem. This source is NOT input to the Stereo-to-Mono mixer. The maximum allowable input is 1 V_{RMS} (sinusoidal). This input is internally biased at the Vrefout voltage reference and requires AC coupling to external circuitry. If this input is not used, it should be connected to the Vrefout pin or AC coupled to Analog ground.

PHONE - Analog Mono Source, Input

This signal is generally used as a voice modem connection to the audio subsystem. This source is NOT input to the Stereo-to-Mono mixer. The maximum allowable input is 1 V_{RMS} (sinusoidal). This input is internally biased at the Vrefout voltage reference and requires AC coupling to external circuitry. If this input is not used, it should be connected to the Vrefout pin or AC coupled to analog ground.

MIC1 - Analog Mono Source, Input

This analog input is a monophonic source to the analog output mixer. It is generally used as a desktop microphone connection to the audio subsystem. This input is MUX-selectable to the input mixer with the MIC2 input source. The maximum allowable input is 1 V_{RMS} (sinusoidal). This input is internally biased at the Vrefout voltage reference and requires AC coupling to external circuitry. If this input is not used, it should be AC coupled to analog ground.

MIC2 - Analog Mono Source, Input

This analog input is a monophonic source to the analog output mixer. It is generally used as an alternate microphone connection to the audio subsystem. This input is MUX-selectable to the input mixer with the MIC1 input source. The maximum allowable input is 1 V_{RMS} (sinusoidal). This input is internally biased at the Vrefout voltage reference and requires AC coupling to external circuitry. If this input is not used, it should be AC coupled to analog ground.

LINE_IN_L and LINE_IN_R- Analog Line Source, Inputs

These inputs form a stereo input pair to the Codec. The maximum allowable input is 1 V_{RMS} (sinusoidal). These inputs are internally biased at the Vrefout voltage reference. AC coupling to external circuitry is required. If these inputs are not used, they should both be connected to the Vrefout pin or both AC coupled, with separate AC coupling caps, to analog ground.

CD_L and CD_R - Analog CD Source, Inputs

These inputs form a stereo input pair. Generally used for the Redbook CD audio connection to the audio subsystem. The maximum allowable input is 1 V_{RMS} (sinusoidal). These inputs are internally biased at the Vrefout voltage reference. AC coupling to external circuitry is required. If these inputs are not used, they should both be connected to the Vrefout pin or both AC coupled, with separate AC coupling caps, to analog ground.

CD_GND - Analog CD Common Source, Input

This analog input is used to remove common mode noise from Redbook CD audio signals. The impedance on the input signal path should be one half the impedance on the CD_L and CD_R input paths. This pin requires AC coupling to external circuitry. If this input is not used, it should be connected to the Vrefout pin or AC coupled to analog ground.

VIDEO_L and VIDEO_R - Analog Video Audio Source, Inputs

These inputs form a stereo input pair. It is generally used for the audio signal output of a video device. The maximum allowable input is 1 V_{RMS} (sinusoidal). These inputs are internally biased at the Vrefout voltage reference. AC coupling to external circuitry is required. If these inputs are not used, they should both be connected to the Vrefout pin or both AC coupled, with separate AC coupling caps, to analog ground.

AUX_L and AUX_R - Analog Auxiliary Source, Inputs

These inputs form a stereo input pair. The maximum allowable input is 1 V_{RMS} (sinusoidal). These inputs are internally biased at the Vrefout voltage reference. AC coupling to external circuitry is required. If these inputs are not used, they should both be connected to the Vrefout pin or both AC coupled, with separate AC coupling caps, to analog ground.

LINE_OUT_L and LINE_OUT_R - Analog Line Level Outputs

These signals are analog outputs from the stereo output mixer. The full scale output voltage for output is nominally 1 V_{RMS} and is internally biased at the Vrefout voltage reference. It is required to either AC couple these pins to external circuitry or DC couple them to a buffer op-amp biased at the Vrefout voltage. These pins need a 680 pF to 1000 pF NPO capacitor attached to analog ground.

ALT_LINE_OUT_L and ALT_LINE_OUT_R - Analog Alternate Line Level Outputs

These signals are analog outputs from the stereo output mixer. The full scale output voltage for each output is nominally 1 V_{RMS} and is internally biased at the Vrefout voltage reference. It is required to either AC couple these pins to external circuitry or DC couple them to a buffer op-amp biased at the Vrefout voltage. These pins need a 680 pF to 1000 pF NPO capacitor attached to analog ground.

MONO_OUT, Analog Mono Line Level Output

This signal is an analog output from the Mono output mixer or MIC1/2. When the Mono output mixer is selected, the left and right channels are mixed from the output of the stereo input mixer. When the MIC mode is selected, MIC1 or MIC2 is routed to the Mono_Out. The full scale output is nominally 1 V_{RMS} and is internally biased at the Vrefout voltage reference. AC coupling to external circuitry is required. This pin needs a 680 pF to 1000 pF NPO capacitor attached to analog ground.

Filter and Reference Pins

REFFLT - Internal Reference Voltage, Input

This is the voltage reference used internal to the part. A 0.1 µF and a 1 µF (must not be larger than 1 µF) capacitor with short, wide traces must be connected to this pin. No other connections should be made to this pin.

Vrefout - Voltage Reference, Output

All analog inputs and outputs are centered around Vrefout which is nominally 2.2 Volts. This pin may be used to level shift external circuitry, however any external loading should be buffered.

AFLT1 - Left Channel Antialiasing Filter Input

This pin needs a 1000 pF NPO capacitor attached to analog ground.

AFLT2 - Right Channel Antialiasing Filter Input

This pin needs a 1000 pF NPO capacitor attached to analog ground.

FLTI - FLTO - 3D Filter

A 1000 pF capacitor must be attached between FLTI and FLTO if the 3D function is used.

FLT3D - 3D Filter

A 0.01 µF capacitor must be attached from this pin to AGND if the 3D function is used.

Power Supplies

DVdd1, DVdd2 - Digital Supply Voltage

Digital supply voltage for the AC-link section of the Codec. These pins can be tied to +5 V digital or to +3.3 V digital. The Codec and Controller's AC-link should share a common digital supply

DVss1, DVss2 - Digital Ground

Digital ground connection for the AC-link section of the Codec. These pins should be isolated from analog ground currents.

AVdd1, AVdd2 - Analog Supply Voltage

Analog supply voltage for the analog and mixed signal sections of the Codec. These pins must be tied to +5 Volt power supply. It is strongly recommended that +5 Volts be generated from a voltage regulator to ensure proper supply currents and noise immunity from the rest of the system.

AVss1, AVss2 - Analog Ground

Ground connection for the analog, mixed signal, and substrate sections of the Codec. These pins should be isolated from digital ground currents.

9.0 PARAMETER AND TERM DEFINITIONS

AC '97 Specification

Refers to the *Audio Codec '97 Component Specification Ver 2.1* published by Intel® Corporation [1].

AC '97 Controller or Controller

Refers to the control chip which interfaces to the Codec's AC-link. This has been also called *DC '97* for Digital Controller '97 [1].

AC '97 Registers or Codec registers

Refers to the 64-field register map defined in the AC '97 Specification.

ADC

Refers to a single Analog-to-Digital converter in the Codec. "ADCs" refers to the stereo pair of Analog-to-Digital converters.

DAC

A single Digital-to-Analog converter in the Codec "DACs" refers to the stereo pair of Digital-to-Analog converters.

Codec

Refers to the chip containing the ADCs, DACs, and analog mixer. In this data sheet, the Codec is the CS4297A.

FFT

Fast Fourier Transform.

Resolution

The number of bits in the output words to the DACs, and in the input words to the ADCs.

Differential Nonlinearity

The worst case deviation from the ideal code width. Units in LSB.

dB FS A

dB FS is defined as dB relative to full-scale. The "A" indicates an A weighting filter was used.

Frequency Response (FR)

FR is the deviation in signal level verses frequency. The 0 dB reference point is 1 kHz. The amplitude corner, Ac, lists the maximum deviation in amplitude above and below the 1 kHz reference point. The listed minimum and maximum frequencies are guaranteed to be within the Ac from minimum frequency to maximum frequency inclusive.

Dynamic Range (DR)

DR is the ratio of the RMS full-scale signal level divided by the RMS sum of the noise floor, in the presence of a signal, available at any instant in time (no change in gain settings between measurements). Measured over a 20 Hz to 20 kHz bandwidth with units in dB FS A.

Total Harmonic Distortion plus Noise (THD+N)

THD+N is the ratio of the RMS sum of all non-fundamental frequency components, divided by the RMS full-scale signal level. It is tested using a -3 dB FS input signal and is measured over a 20 Hz to 20 kHz bandwidth with units in dB FS.

Signal to Noise Ratio (SNR)

SNR, similar to DR, is the ratio of an arbitrary sinusoidal input signal to the RMS sum of the noise floor, in the presence of a signal. It is measured over a 20 Hz to 20 kHz bandwidth with units in dB.

S/PDIF

Sony/Phillips Digital Interface. This interface was established as a means of digitally interconnecting consumer audio equipment. The documentation for S/PDIF has been superseded by the IEC-958 consumer digital interface document.

Interchannel Isolation

The amount of 1 kHz signal present on the output of the grounded AC-coupled line input channel with 1 kHz, 0 dB, signal present on the other line input channel. Units in dB.

Interchannel Gain Mismatch

For the ADCs, the difference in input voltage to get an equal code on both channels. For the DACs, the difference in output voltages for each channel when both channels are fed the same code. Units in dB.

PATHS

A-D: Analog in, through the ADC, onto the serial link.

D-A: Serial interface inputs through the DAC to the analog output.

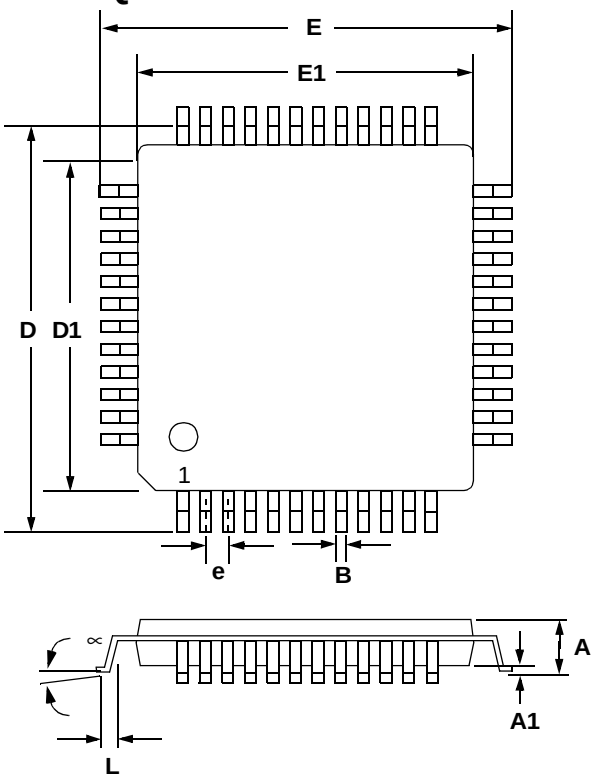
A-A: Analog in to Analog out (analog mixer).

10.0 REFERENCES

1) Intel, Audio Codec '97 Component Specification, Revision 2.1, May 22,1998.
http://developer.intel.com/pc-supp
/platform/ac97/

11.0 PACKAGE DIMENSIONS

48L TQFP PACKAGE DRAWING



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	----	0.063	----	1.600
A1	0.002	0.006	0.050	0.150
B	0.007	0.011	0.170	0.270
D	0.343	0.366	8.700	9.300
D1	0.272	0.280	6.900	7.100
E	0.343	0.366	8.700	9.300
E1	0.272	0.280	6.900	7.100
e*	0.016	0.024	0.400	0.600
L	0.018	0.030	0.450	0.750
∝	0.000°	7.000°	0.000°	7.000°

* Nominal pin pitch is 0.50 mm

Controlling dimension is mm.
JEDEC Designation: MS026

• Notes •

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