WM9704Q

4-Channel Surround Sound Codec

Production Data, February 2000, Rev 2.1

DESCRIPTION

WM9704Q is a high quality audio codec compliant with the AC'97 Revision 2.1 specification. It performs full duplex 18-bit codec functions from 8 to 48k samples/s and offers excellent quality with high SNR. Features include 3D sound and line-level outputs. Support is also provided for variable sample rates and master/slave mode operation. Additionally the WM9704Q provides two proprietary modes:

4-channel quad mode enables two channels of ADC and DAC plus an additional two DAC channels as rear outputs.

6-channel mode configures the device to provide external support for two additional stereo outputs via the GPIO pins.

WM9704Q is interchangeable with AC'97 Codecs from Wolfson and other suppliers in the basic Revision 2.1 mode. WM9704Q is fully operable with 3.3V or 5.0V or mixed 3.3/5.0V supplies and is packaged in an industry standard 48-pin TQFP package.

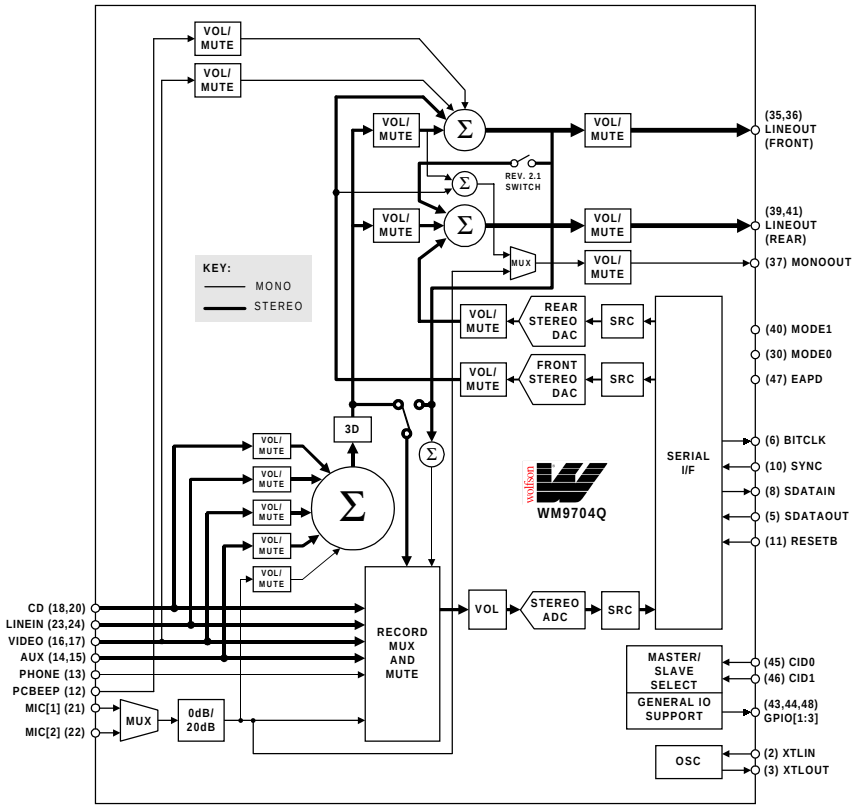
FEATURES

- 4 DAC channels, stereo ADC
- Balanced mixer architecture
- S/N ratio > 95dB
- Variable rate audio and modem support
- Analogue 3D stereo enhancement
- Line level outputs
- Master/slave ID selection
- Low power implementation
- 3.3V or 5V operation
- 48-pin TQFP package

APPLICATIONS

- 4-channel surround sound solution implemented with 2 additional internal DACs
- 6-channel surround sound supported via connection of a stereo DAC (WM8725) to GPIO pins
- Supports 4-channel playback of analogue sources such as CD

BLOCK DIAGRAM



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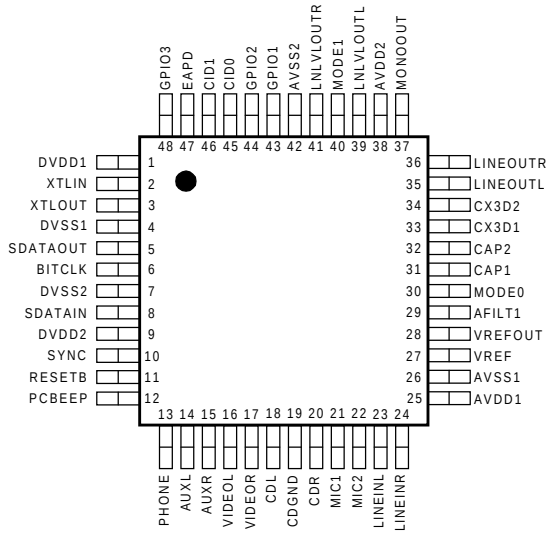
PIN CONFIGURATION



ORDERING INFORMATION

DEVICE	TEMP. RANGE	PACKAGE
WM9704CFT/V	0 to 70°C	48-pin TQFP

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

As per JEDEC specifications A112-A and A113-B, this product requires specific storage conditions prior to surface mount assembly. It has been classified as having a Moisture Sensitivity Level of 2 and as such will be supplied in vacuum-sealed moisture barrier bags.

CONDITION	MIN	MAX
Digital supply voltage	-0.3V	+7V
Analogue supply voltage	-0.3V	+7V
Voltage range digital inputs	DVSS -0.3V	DVDD +0.3V
Voltage range analogue inputs	AVSS -0.3V	AVDD +0.3V
Operating temperature range, T_A	0°C	+70°C
Storage temperature	-65°C	+150°C
Package body temperature (soldering 10 seconds)		+240°C
Package body temperature (soldering 2 minutes)		+183°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital supply range	DVDD1, DVDD2		-10%	3.3 to 5.0	+10%	V
Analogue supply range	AVDD1, AVDD2		-10%	3.3 to 5.0	+10%	V
Digital ground	DVSS1, DVSS2			0		V
Analogue ground	AVSS1, AVSS2			0		V
Difference DVSS to AVSS			-0.3	0	+0.3	V
Analogue supply current		DVDD, AVDD = 5V		35		mA
Digital supply current		DVDD, AVDD = 5V		25		mA
Standby supply current (all PRs set)		DVDD, AVDD = 5V		10		µA
Analogue supply current		DVDD, AVDD = 3.3V		22		mA
Digital supply current		DVDD, AVDD = 3.3V		15		mA
Standby supply current (all PRs set)		DVDD, AVDD = 3.3V		6		µA

ELECTRICAL CHARACTERISTICS

Test Characteristics:
AVDD = 5V, GND = 0V ……..T_A = 0°C to +70°C, unless otherwise stated
DVDD = 3.3V, GND = 0V ……..T_A = 0°C to +70°C, unless otherwise stated

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital Logic Levels (DVDD = 3.3 or 5.0V)						
Input LOW level	V_{IL}		AVSS -0.3		0.8	V
Input HIGH level	V_{IH}		2.2		AVDD +0.3	V
Output LOW	V_{OL}				0.1 x DVSS	V
Output HIGH	V_{OH}		0.9 x DVDD			V
Analogue I/O Levels (Input Signals on any inputs, Outputs on LINEOUT L, R and MONO)						
Input level		Minimum input impedance = 10k	AVSS -100mV		AVDD +100mV	V
Output level		Into 10kohm load	AVSS +100mV	Near rail to rail	AVDD -100mV	V
Reference Levels						
Reference input/output	CAP2		2/5 AVDD	AVDD/2	3/5 AVDD	V
CAP2 impedance				75		kohms
Mixer reference	VREF			Buffered CAP2		V
MIC reference	VREFOUT			Buffered CAP2		V
ADC reference	CAP1			Buffered CAP2		V
DAC reference	AFILT1			Buffered CAP2		V
MIDBUFF current sink (pins CAP1, AFILT2, VREF and VREFOUT)		AVDD = 5V	-5	-15		mA
MIDBUFF current source (pins CAP1, AFILT1, VREF and VREFOUT)		AVDD = 5V	5	15		mA
MIDBUFF current source (pins CAP1, AFILT1, VREF and VREFOUT)		AVDD = 3.3V		5		mA

Test Characteristics:
AVDD = 5V, GND = 0V ……..T_A = 0°C to +70°C, unless otherwise stated
DVDD = 3.3V, GND = 0V ……..T_A = 0°C to +70°C, unless otherwise stated

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DAC Circuit Specifications (AVDD = 5V) 48kHz sampling						
SNR A-weighted (Note 1)			85	96		dB
Full scale output voltage		V_{REF} = 2.5V		1.0		Vrms
THD		-3dBFS input	74	90		dB
Frequency response			20		19,200	Hz
Transition band			19,200		28,800	Hz
Stop band			28,800			Hz
Out of band rejection				-40		dB
Spurious tone reduction				-100		dB
PSRR		20 to 20kHz		40		dB
ADC Circuit Specifications (AVDD = 5V) 48kHz sampling						
SNR A-weighted (Note 1)			75	85		dB
ADC input for full scale output		V_{REF} = 2.5V		1.0		Vrms
THD		-6dBV input	74	90		dB
Frequency response			20		19,200	Hz
Transition band			19,200		28,800	Hz
Stop band			28,800			Hz
Stop band rejection			-74			dB
PSRR		20 to 20kHz		40		dB
Mixer Circuit Specifications (AVDD = 5V) 48kHz sampling						
SNR CD path A-weighted (Note 1)			90	100		dB
SNR Other paths A-weighted (Note 1)			85	95		dB
Maximum input voltage			AVSS	1.0	AVDD	Vrms
Maximum output voltage on LINEOUT			1.0	1.8		Vrms
THD		0dBV input	74	90		dB
Frequency response (+/-1dB)			20		20,000	Hz
Input impedance (CD inputs)		At any gain	10	15		kohm
Input impedance (other mixer inputs)		At max gain	10	20		kohm
		At 0db gain		100		kohm
Input impedance MIC inputs		At max gain		80		kohm
		At 0db gain	10	15		kohm
PSRR		20 to 20kHz		40		dB
DAC Circuit Specifications (AVDD = 3.3V) 48kHz sampling						
SNR A-weighted (Note 1)				96		dB
Full scale output voltage		V_{REF} = 1.65V		0.7		Vrms
THD		-3dBFS input		90		dB
Frequency response			20		19,200	Hz
Transition band			19,200		28,800	Hz
Stop band			28,800			Hz
Out of band rejection				-40		dB
Spurious tone reduction				-100		dB
PSRR		20 to 20kHz		40		dB

Test Characteristics:
AVDD = 5V, GND = 0V ……..T_A = 0°C to +70°C, unless otherwise stated
DVDD = 3.3V, GND = 0V ……..T_A = 0°C to +70°C, unless otherwise stated

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADC Circuit Specifications (AVDD = 3.3V) 48kHz sampling						
SNR A-weighted (Note 1)				82		dB
ADC input for full scale output		V_{REF} = 1.65V		0.7		Vrms
THD		-9dBV input		80		dB
Frequency response			20		19,200	Hz
Transition band			19,200		28,800	Hz
Stop band			28,800			Hz
Stop band rejection			-74			dB
PSRR		20 to 20kHz		40		dB
Mixer Circuit Specifications (AVDD = 3.3V) 48kHz sampling						
SNR CD path A-weighted (Note 1)				97		dB
SNR Other paths A-weighted (Note 1)				92		dB
Maximum input voltage				0.7		Vrms
Maximum output voltage on LINEOUT				0.7		Vrms
THD		-3dBV input		90		dB
Frequency response (+/-1dB)			20		20,000	Hz
Input impedance (CD inputs)		At any gain		15		kohm
Input impedance (other Mixer inputs)		At max gain		20		kohm
		At 0db gain		100		kohm
Input impedance MIC inputs		At max gain		80		kohm
		At 0db gain		15		kohm
PSRR		20 to 20kHz		40		dB
Clock Frequency Range						
Crystal clock				24.576		MHz
BIT_CLK frequency				12.288		MHz
SYNC frequency				48.0		kHz

Note:

1. SNR is the ratio of 0dB signal output level to the output level with no signal, measured A-weighted over a 20Hz to 20kHz bandwidth.

PIN DESCRIPTION

PIN	NAME	TYPE	DESCRIPTION
1	DVDD1	Supply	Digital positive supply
2	XTLIN	Digital input	Clock crystal connection or clock input (XTAL not used)
3	XTLOUT	Digital output	Clock crystal connection
4	DVSS1	Supply	Digital ground supply
5	SDATAOUT	Digital input	Serial data input
6	BITCLK	Digital output	Serial interface clock output to AC'97 controller
7	DVSS2	Supply	Digital ground supply
8	SDATAIN	Digital output	Serial data output to AC'97 controller
9	DVDD2	Supply	Digital positive supply
10	SYNC	Digital input	Serial interface sync pulse from AC'97 controller
11	RESETB	Digital input	NOT reset input (active low, resets registers)
12	PCBEEP	Analogue input	Mixer input, typically for PCBEEP signal
13	PHONE	Analogue input	Mixer input, typically for PHONE signal
14	AUXL	Analogue input	Mixer input, typically for AUX signal
15	AUXR	Analogue input	Mixer input, typically for AUX signal
16	VIDEOL	Analogue input	Mixer input, typically for VIDEO signal
17	VIDEOR	Analogue input	Mixer input, typically for VIDEO signal
18	CDL	Analogue input	Mixer input, typically for CD signal
19	CDGND	Analogue input	CD input common mode reference (ground)
20	CDR	Analogue input	Mixer input, typically for CD signal
21	MIC1	Analogue input	Mixer input with extra gain if required
22	MIC2	Analogue input	Mixer input with extra gain if required
23	LINEINL	Analogue input	Mixer input, typically for LINE signal
24	LINEINR	Analogue input	Mixer input, typically for LINE signal
25	AVDD1	Supply	Analogue positive supply
26	AVSS1	Supply	Analogue ground supply, chip substrate
27	VREF(1)	Analogue output	Buffered CAP2
28	VREFOUT	Analogue output	Reference for microphones; buffered CAP2
29	AFILT1(1)	Analogue output	Buffered CAP2
30	MODE0	Digital input	Mode select pin, internal pull down (6-channel support I^2S enable)
31	CAP1(1)	Analogue output	Buffered CAP2
32	CAP2	Analogue input	Reference input/output; pulls to midrail if not driven
33	CX3D1	Analogue output	Output pin for 3D difference signal
34	CX3D2	Analogue input	Input pin for 3D difference signal
35	LINEOUTL	Analogue output	Main analogue output for left channel
36	LINEOUTR	Analogue output	Main analogue output for right channel
37	MONOOUT	Analogue output	Main mono output
38	AVDD2	Supply	Analogue positive supply
39	LNLVLOUTL	Analogue output	Left channel line level output
40	MODE1	Digital input	Mode select pin, internal pull down (Quad mode select)
41	LNLVLOUTR	Analogue output	Right channel line level output
42	AVSS2	Supply	Analogue ground supply, chip substrate
43	GPIO1	Programmable I/O	GPIO or I^2S
44	GPIO2	Programmable I/O	GPIO or I^2S
45	CID0	Digital input	Master/slave ID select (internal pull-up)
46	CID1	Digital input	Master/slave ID select (internal pull-up)
47	EAPD	Digital output	External amplifier power down/GPO
48	GPIO3	Programmable I/O	GPIO or I^2S

Note:

1. Pins 27, 29 and 31 have an internal connection.

DETAILED TIMING DIAGRAMS

Test Characteristics:
AVDD = 5V, GND = 0V ……..T_A = 0°C to +70°C, unless otherwise stated
DVDD = 3.3V, GND = 0V ……..T_A = 0°C to +70°C, unless otherwise stated
All measurements are taken at 10% to 90% VDD, unless otherwise stated.

AC-LINK LOW POWER MODE

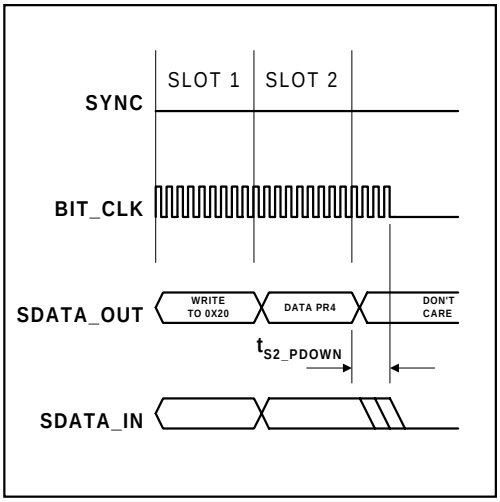


Figure 1 AC-Link Powerdown Timing

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
End of slot 2 to BITCLK SDATIN low	t_{S2_PDOWN}			1.0	µs

COLD RESET

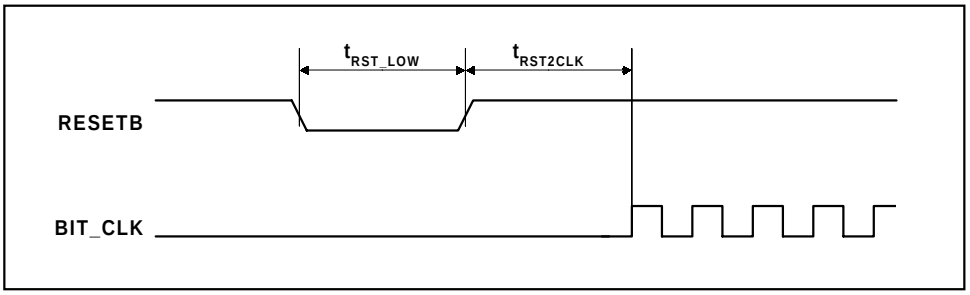


Figure 2 Cold Reset Timing

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
RESETB active low pulse width	t_{RST_LOW}	1.0			µs
RESETB inactive to BIT_CLK startup delay	t_{RST2_CLK}	162.8			ns

WARM RESET

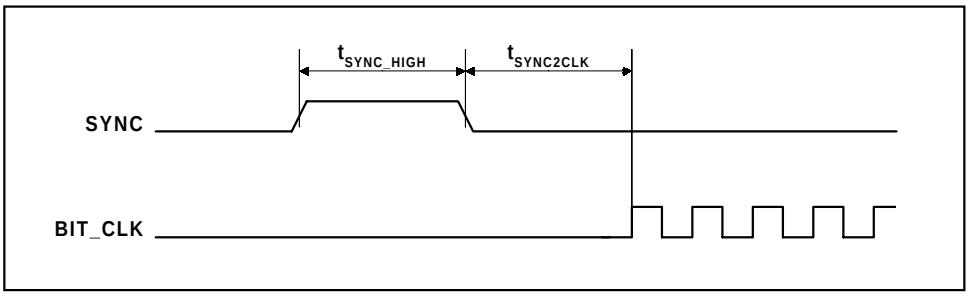


Figure 3 Warm Reset Timing

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
SYNC active high pulse width	t_{SYNC_HIGH}		1.3		µs
SYNC inactive to BIT_CLK startup delay	t_{SYNC2_CLK}	162.4			ns

CLOCK SPECIFICATIONS

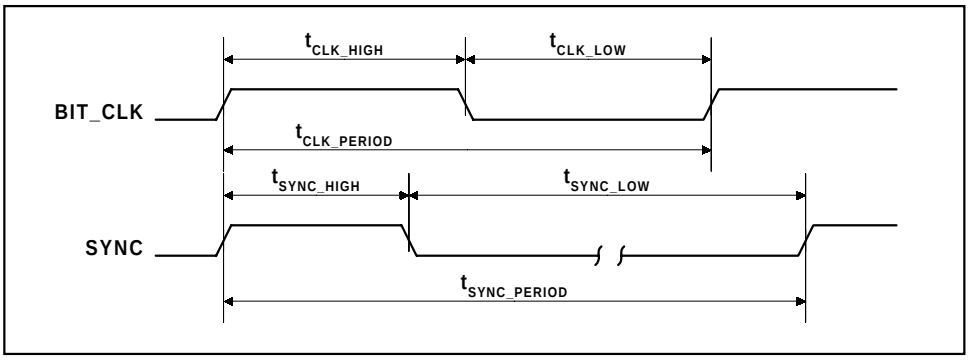


Figure 4 Clock Specifications (50pF External Load)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
BIT_CLK frequency			12.288		MHz
BIT_CLK period	t_{CLK_PERIOD}		81.4		ns
BIT_CLK output jitter				750	ps
BIT_CLK high pulse width (Note 1)	t_{CLK_HIGH}	32.56	40.7	48.84	ns
BIT_CLK low pulse width (Note 1)	t_{CLK_LOW}	32.56	40.7	48.84	ns
SYNC frequency			48.0		KHz
SYNC period	t_{SYNC_PERIOD}		20.8		µs
SYNC high pulse width	t_{SYNC_HIGH}		1.3		µs
SYNC low pulse width	t_{SYNC_LOW}		19.5		µs

Note: Worst case duty cycle restricted to 40/60

DATA SETUP AND HOLD (50pF EXTERNAL LOAD)

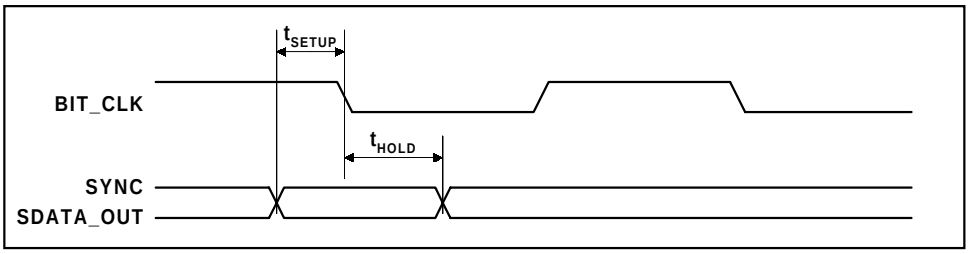


Figure 5 Data Setup and Hold (50pF External Load)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Setup to falling edge of BIT_CLK	t_{SETUP}	15.0			ns
Hold from falling edge of BIT_CLK	t_{HOLD}	5.0			ns

Note: Setup and hold time parameters for SDATA_IN are with respect to AC'97 Controller.

SIGNAL RISE AND FALL TIMES

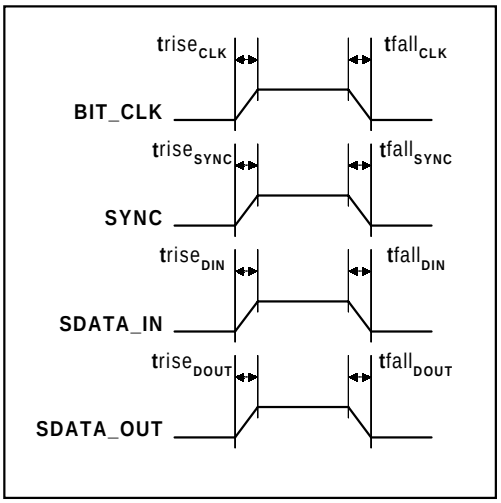


Figure 6 Signal Rise and Fall Times (50pF external load)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
BIT_CLK rise time	$trise_{CLK}$	2		6	ns
BIT_CLK fall time	$tfall_{CLK}$	2		6	ns
SYNC rise time	$trise_{SYNC}$	2		6	ns
SYNC fall time	$tfall_{SYNC}$	2		6	ns
SDATA_IN rise time	$trise_{DIN}$	2		6	ns
SDATA_IN fall time	$trise_{DIN}$	2		6	ns
SDATA_OUT rise time	$trise_{DOUT}$	2		6	ns
SDATA_OUT fall time	$tfall_{DOUT}$	2		6	ns

SYSTEM INFORMATION

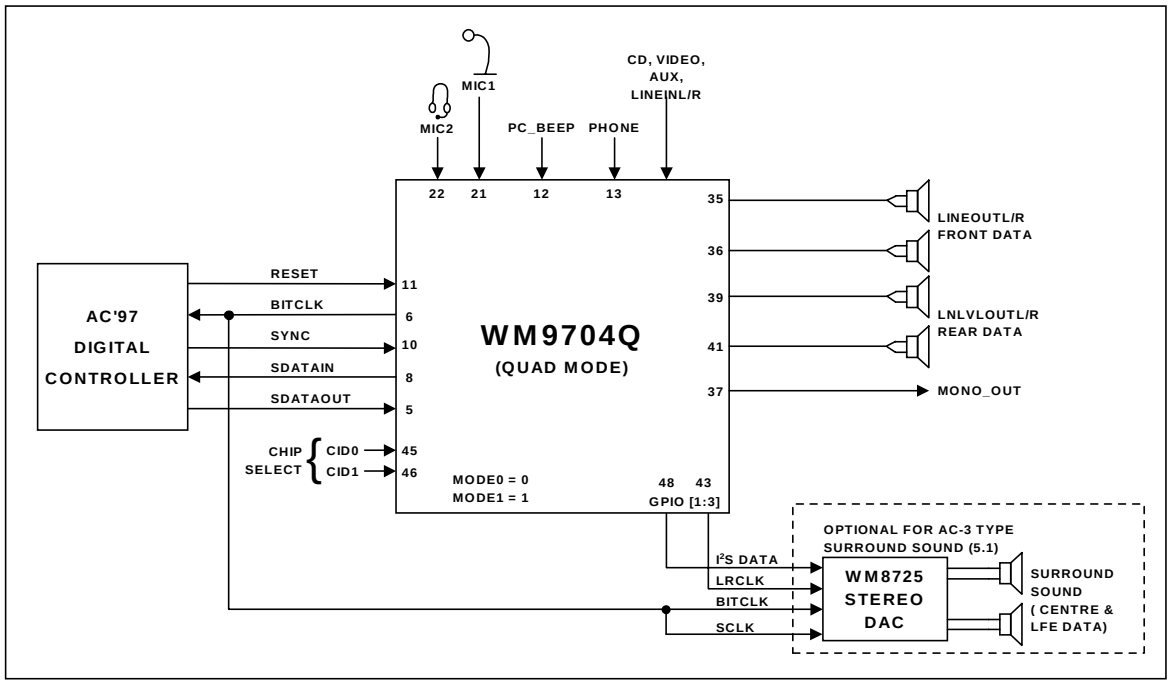


Figure 7 WM9704Q in Typical Quad Mode Application

DEVICE DESCRIPTION

INTRODUCTION

The WM9704Q Codec comprises two channels of ADC and four channels of DAC. This enables a four channel surround sound solution to be implemented (Quad mode). A symmetric mixer is provided which allows analogue signals such as CD inputs to be mixed into both front and rear channel paths simultaneously.

Alternatively, the device can be configured in 6-channel I^2S mode. In this mode the device uses three GPIO pins to output rear channel and centre and LFE data in I^2S format to an external DAC (WM8725) to build a full 6 channel surround sound solution.

The WM9704Q can also be configured as a standard AC'97 Revision 2.1 compliant device, including line level outputs and with support for the variable rate audio sample rates (2 channel mode).

The WM9704Q comprises a stereo 18-bit Codec, (that is, 2 ADCs and 2 DACs) plus two additional DACs. The WM9704Q also has a comprehensive analogue mixer with 4 sets of stereo inputs, plus phone, 2 microphone, and PC-beep inputs. On-chip reference circuits generate the necessary bias voltages for the device, and a bi-directional serial interface allows transfer of control data and DAC and ADC words to and from the AC'97 controller. The WM9704Q supports 18-bit resolution within the DAC and ADC functions, but the AC'97 serial interface specification allows any word length up to 20-bits to be written to, or read from, the AC'97 Codec. These words are MSB justified, and any LSBs not used will simply default to 0. Normally it is anticipated that 16-bit words will be used in most PC type systems. Therefore, for the DAC, 16-bit words will be downloaded into the Codec from the controller, along with padding of 0s to make the 16-bit word up to 20-bit length. In this case, the WM9704Q will process the 16-bit word along with 0 padding bits in the 2 LSB locations (to make 18-bit). At the ADC output, WM9704Q will provide an 18-bit word, again with 0s in the two LSB locations (20-bit). The AC'97 controller will then ignore the 4 LSBs of the 20-bit word. When the WM9704Q is interrogated, it responds indicating it is an 18-bit device.

The WM9704Q has the ADC and DAC functions implemented using oversampled, or sigma-delta converters, and uses on-chip digital filters to convert these 1-bit signals to and from the 48ks/s 16/18-bit PCM words that the AC'97 controller requires. The digital parts of the device are powered separately from the analogue to optimise performance, and 3.3V digital and 5V analogue supplies may be used on the same device to further optimise performance. Digital IOs are 5V tolerant when the analogue supplies are 5V, so the WM9704Q may be connected to a controller running on 5V supplies, but use 3.3V for the digital section of WM9704Q. WM9704Q is also capable of operating with a 3.3V supply only (digital and analogue).

An internally generated midrail reference is provided at pin CAP2 which is used as the chip reference. This pin should be heavily decoupled.

Additional features added to the Intel AC'97 specification, such as the EAPD (External Amplifier Power Down) bit, internal connection of PC-beep to the outputs in the case where the device is reset, are supported, along with optional features such as variable sample rate support.

OPERATIONAL MODES

The WM9704Q is pin programmable to operate in the following modes:

MODE1 PIN	MODE0 PIN	OPERATIONAL MODE	RESULTING DEVICE BEHAVIOUR
0	0	2-channel	Rev 2.1 compliant codec (2-channel mode)
0	1	6-channel I^2S	Rev 2.1 compliant codec (6-channel mode)
1	0	Quad mode	Quad DAC mode (with I^2S 6-channel support)

Table 1 Operating Modes

QUAD MODE

In this mode the additional 2 DAC channels are enabled, using the line level output pins 39 and 41 as outputs. An additional mixer block in this path allows the analogue mix, excluding the front DAC channels, to be summed into the rear channel mix. Additional gain controls (PGAs) are provided to allow adjustment of front and rear mix levels separately (registers 72h and 74h) prior to summing the analogue mix to these channels. The rear channel DACs also are gain adjustable using register 70h. This function duplicates the features that are provided for the front DAC channel (gain range, step size etc).

Features in this mode are as follows:

- Vendor ID reads back WML4.
- All 6 audio channels are flagged as supported (if I^2S enable bit is set).
- Headphone channel flagged as not supported (bit ID4 in register 00h).
- 4 channels of DAC and 2 of ADC conversion available, with all recommended Audio and modem sample rates supported via the audio sample rate registers 2Ch (front channels; slots 3 and 4), 2Eh (rear channels; slots 7 and 8) and 32h (ADCs) (Note if ID is selected as 11, register 30h is used for sample rate of LFE channel; slot 9).
- GPIO capability supporting Bits 11 to 13 is flagged as supported.
- Master/slave ID0/1 are supported, with automatic re-mapping of the rear or LFE/centre DAC slot data onto the rear DACs when ID 10 or 11 are selected (normally surround slots are mapped onto the rear DACs).
- LFE and Center channel data, plus a duplicate of the rear channel data, is sent from the GPIO pins in I^2S format, at 48ks/s rate (no variable rates supported by the I^2S outputs).
- Headphone/line level outputs are used to output the rear DAC and mixer channel, with volume controlled from register 38h.
- Wolfson 3D stereo enhancement supported.
- Master volume control register maps to the location dependant on selected ID: (ID 00 or 01 uses master volume at register 02h, ID 10 uses 38h (surround volume) and ID11 uses 36h (LFE, Center volume) In this case, bits 7 and 15 act as left and right mute.).
- DAC mute (reg18h) automatically de-muted, when ID is 1x, i.e. used as surround DAC or LFE/center, when surround or LFE/center master volume is de-muted.
- In order to achieve the above functionality, the following changes to the Revision 2.1 compliant defaults are made.
- Revision 2.1 legacy compliance switch is opened (can be closed using REV2SW bit in register 5Ah).
- Rear channel mixer PGA default is now not-muted, 0dB gain (same as front channel mixer).
- LNLVL pin volume control is now controlled from 02h unless ID=IO when volume control is from 38h.
- Rear DAC level set by register 70h, default is 0dB not-muted.
- Front mixer and rear mixer gains set in registers 72h and 74h.

REVISION 2.1 COMPLIANT 6-CHANNEL I^2S MODE

In this mode the device now has 6-channel support and GPIO capability. Rear and LFE centre DAC data is mapped onto the GPIO output pins as I^2S data when these data slots are tagged as valid, and the I^2S enable bit is set in register 5Ah. Enabling of I^2S overrides the GPIO function.

Features in this mode are as follows:

- Vendor ID reads back as WML3.
- 2 channels of ADC and DAC conversion provided.
- Rear and LFE/centre DAC slots are flagged as supported in extended audio capability register 28h.
- GPIO capability supporting bits 11-13 is flagged as supported.
- Master/slave ID0/1 are supported.
- Surround audio data not sent to the DACs is sent from the GPIO pins in I^2S format, at 48ks/s rate (no variable rates supported by the I^2S outputs).
- Headphone/line level outputs duplicating the main outputs are supported, with gain control from register 04h.
- Wolfson 3D stereo enhanced sound supported.
- Master volume control register maps to the location dependant on selected ID: (ID 00 or 01 uses master volume at register 02h, ID 10 uses 38h (surround volume) and ID11 uses 36h (LFE, Centre volume) In this case, bits 7 and 15 act as left and right mute.).

REVISION 2.1 COMPLIANT 2-CHANNEL MODE

Features in this mode are as follows:

- Vendor ID reads back as WML3.
- 2 channels of ADC and DAC conversion provided, with all recommended audio and modem sample rates supported via the audio sample rate registers 2Ch and 32h.
- Master/slave ID0/1 are supported.
- Headphone/line level outputs duplicating the main outputs, are supported, with gain control from register 04h.
- Wolfson 3D stereo enhanced sound supported.
- Master volume control register maps to the location dependant on selected ID: (ID 00 or 01 uses master volume at register 02h, ID 10 uses 38h (surround volume) and ID11 uses 36h (LFE, Centre volume).

GPIO PINS AND I^2S MODE

The AC'97 Revision 2.1 specification allows for provision of programmable IO pins, up to 16 in number. Within the 48-pin TQFP package used, provision has been made for 3 pins to be used as GPIO pins. These pins (numbers 43, 44, 48) are also used as I^2S output pins to support multi-channel operation.

When used as GPIO pins, the pins 43, 44, 48 are mapped respectively onto the bits 11,12,13 in the AC-link slot 12. These optional locations may be configured in any way: as inputs or outputs, supporting interrupt operation etc, offering maximum flexibility to the user. The appropriate GPIO control registers are supported to control these pins.

When used as I2S pins, pin 43 becomes the shared LRCLK, with frequency fixed at 48kHz. Pins 44 and 48 become the output data, clocked out at the BITCLK rate. Thus to connect an external DAC, configure it in I2S mode:

- Connect BITCLK signal from the WM9704Q to the SCLK on the DAC.
- Connect BITCLK from the AC'97 to BCLK on the DAC.
- Connect pin 43 from the WM9704Q to the LRCLK on the DAC.
- Connect one of the two data pins 44 or 48 on WM9704Q to the SDATA pin on the DAC.

Note that the DAC must support serial interface data rates at up to 12.5MHz (Wolfson DACs such as the WM8725 and WM8733 support this).

I2S is enabled when GPIO is not enabled (GPIO Bit 0 = 0, PRA = 1 in register 3Eh), is enabled in register 3Eh) and vendor specific I2S (bit 7) in register 5Ah is set.

The following table shows the connections to a typical I^2S compatible stereo DAC (e.g. WM8725).

WM9704Q CONNECTION	I^2S DAC CONNECTION
BITCLK	SCLK
BITCLK	BLCK
Pin 43 – GPIO1	LRCLK
Pin 44 – GPIO2 (surround data in ID00)	SDATA on other external DAC
	FORMAT pin - connect for I^2S mode
	DEEMPH (if provided) - disable
Pin 48 – GPIO3 (LFE/centre data in ID00)	SDATA on external DAC

Table 2 Connection to External I^2S DACs

Configuration of these pins as GPIO is described in the control interface description.

3D STEREO ENHANCEMENT

This device contains a stereo enhancement circuit, designed to optimise the listening experience when the device is used in a typical PC operating environment. That is, with a pair of speakers placed either side of the monitor with little spatial separation. This circuit creates a difference signal by differencing left and right channel playback data, then filters this difference signal using lowpass and highpass filters whose time constants are set using external capacitors connected to the CX3D pins 33 and 34. Typically the values of 100nF and 47nF set highpass and lowpass poles at about 100Hz and 1kHz respectively. This frequency band corresponds to the range over which the ear is most sensitive to directional effects.

The filtered difference signal is gain adjusted by an amount set using the 4-bit value written to register 22h bits 3 to 0. Value 0h is disable, value Fh is maximum effect. Typically a value of 8h is optimum. The user interface would most typically use a slider type of control to allow the user to adjust the level of enhancement to suit the program material. Bit D13 3D in register 20h is the overall 3D enable bit. The capability register 00h reads back the value 11000 in bits D14 to D10. This corresponds to decimal 24, which is registered with Intel as Wolfson Stereo Enhancement.

Note that the external capacitors setting the filtering poles applied to the difference signal may be adjusted in value, or even replaced with a direct connection between the pins. If such adjustments are made, then the amount of difference signal fed back into the main signal paths may be significant, and can cause large signals which may limit, distort, or overdrive signal paths or speakers. Adjust these values with care, to select the preferred acoustic effect.

There is no provision for pseudo-stereo effects. Mono signals will have no enhancement applied (if the signals are in phase and of the same amplitude).

Signals from the PCM DAC channels do not have stereo enhancement applied. It is assumed that these signals will already have been processed digitally with any required 3D-enhancement effect. Applying the analogue 3D enhancement will corrupt this digital effect. This is equivalent to setting the POP bit in register 20h. As a result, the readback value of this bit is fixed as 1, and attempts to change it will be ignored. POP bit is set to one and cannot be re-set.

VARIABLE SAMPLE RATE SUPPORT

The DACs and ADCs on this device support all the recommended sample rates specified in the Intel Revision 2.1 specification for both audio and modem rates. Default rates are 48ks/s. If alternative rates are selected, the AC'97 interface continues to run at 48k words per second, but data is transferred across the link in bursts such that the net sample rate selected is achieved. It is up to the AC'97 Revision 2.1 compliant controller to ensure that data is supplied to the AC link, and received from the AC link, at the appropriate rate.

The device supports on demand sampling. That is, when the DAC signal processing circuits need another sample, a sample request is sent to the controller which must respond with a data sample in the next frame it sends. For example, if a rate of 24ks/s is selected, on average the device will request a sample from the controller every other frame, for each of the stereo DACs. Note that if an unsupported rate is written to one of the rate registers, the rate will default to the nearest rate supported. The register will then respond when interrogated with the supported rate the device has defaulted to.

ADCs are controlled similarly but with one difference: Normally the left and right channel ADCs sample at the same rate.

AUDIO SAMPLE RATE	CONTROL VALUE D15 TO D0	MODEM SAMPLE RATE	CONTROL VALUE D15 TO D0
		7200	1C20
		8228.57 (57600/7)	2024
8000	1F40	8400	20D0
11025	2B11	9000	2328
16000	3E80	9600	2580
22050	5622	10285.71 (72000/7)	282D
44100	AC44	12000	2EE0
48000	BB80	13714.28 (96000/7)	3592
		19200	4B00
		24000	5DC0

Table 3 Variable Sample Rates Supported

The following table shows which registers control which DAC rates, versus Mode and ID selected

MODE	ID	FRONT DAC RATE REGISTER	REAR DAC RATE REGISTER	ADC RATE REG
Rev 2.1 mode (00)	00 and 01	2Ch		32h
	10	2Eh		
	11	2Ch (centre) and 30h (LFE)		
Rev 2.1 6-channel mode (01)	00 and 01	2Ch		32h
	10	2Eh		
	11	2Ch (centre) and 30h (LFE)		
Quad mode (10)	00 and 01	2Ch	2Eh	32h
	10	2Eh	2Ch	
	11	2Ch (centre) and 30h (LFE)	2Eh	

Table 4 Variable Rate Register Location Versus Mode and ID

GAIN CONTROL REGISTER LOCATION VERSUS MODE AND ID

Depending on what mode and ID the device is operated in, the various gain control registers have locations in the register map that may change. For example, if the Codec is configured as ID 10, it means that the device will be converting the rear surround DAC data. Therefore in this case the surround DAC volume word written to register 38h is now used to control the master volume control, rather than the normal master volume 02h.

In addition, in this case when the surround volume mute control is written as de-mute, then mute in the DAC PGA register 18h is automatically over-ridden, to avoid the user having to make an unexpected additional write to register 18h to de-mute the DAC PGA.

PGA	CODEC ID	REV 2.1 MODE (0X)		QUAD MODE (10)	
		CONTROL REG	MUTE DEFAULT	CONTROL REG	MUTE DEFAULT
Front DAC PGA	0x 10 11	18h	Muted (bit15) AND with 38h,7,15 AND with 36h,7,15	18h	Muted (bit15) AND with 38h,7,15 AND with 36h,7,15
Rear DAC PGA	0x 10 11	70h	Muted (bit15) and powered off	70h	Not-muted (bit15) AND with 02h, 15 AND with 38h,7,15
Front Mixer	0x 10 11	72h	Not-muted (bit15)	72h	Not-muted (bit15)
Rear Mixer	0x 10 11	74h	Permanently muted	74h	Not-muted (bit15)
Front Volume	0x 10 11	02h 38h 36h	Muted (15) muted (7 and 15) muted (7 and 15)	02h 38h 36h	Muted (15) muted (7 and 15) muted (7 and 15)
Rear Volume	0x 10 11	04h	Muted (bit15) Rev 2.1 switch enabled	38h 02h 38h	Muted (7 and 15) muted (15) muted (7 and 15)

Table 5 Gain Control Register Location Versus Mode and ID

MASTER/SLAVE ID0/1 SUPPORT

WM9704Q supports operation as either a master or a slave codec. Configuration of the device as either a master or as a slave, is selected by tying the ID pins CID0 and CID1, pins 45 and 46 on the package.

Fundamentally, a device identified as a master (ID = 00) produces BITCLK as an output, whereas a slave (any other ID) must be provided with BITCLK as an input. This has the obvious implication that if the master device on an AC link is disabled, the slave devices cannot function.

The AC'97 Revision 2.1 specification defines that the ID pins have inverting sense, and are provided with internal weak pull ups. Therefore, if no connections are made to the CID0/1 pins, then the pins pull hi and an ID = 00 is selected, i.e. master. External connects to ground will select other IDs.

PIN 46 CID1	PIN 45 CID0	ID SELECTED	MASTER OR SLAVE	BITCLK
NC	NC	00	Master	Output
NC	Ground	01	Slave	Input
Ground	NC	10	Slave	Input
Ground	Ground	11	Slave	Input

Table 6 ID Selection

WM9704Q supports the AMAP function whereby selection of an ID will automatically map the data from the interface onto the PCM DACs.

CODEC ID	AC–LINK FRAME DATA USED FOR DACS		COMMENTS
	PCM left DAC uses data from slot no.	PCM right DAC uses data from slot no.	
00	3	4	Original definition (master)
01	3	4	Original definition (docking)
10	7	8	Left/right surround channels
11	6	9	Centre/LFE channels
The Codec ID is available to the controller via registers 28h and C3, bits D15 and D14			

Table 7 Default Slot to DAC Mappings Based on Codec ID

The above automatic mapping of data to slots is extended when the device is operated in the alternative modes selectable via the mode pins. In these cases the selection of which data slots are mapped onto internal DACs or I^2S outputs is selectable as follows. (Note I^2S enable bit must be set).

MODE	CODEC ID	SLOTS MAPPED TO FRONT DACS	SLOTS MAPPED TO REAR DACS	DATA TO I^2S D0 PIN 44	DATA TO I^2S D1 PIN 48
Rev 2.1 (00)	00 or 01	3 and 4	Not supported in this mode	Not supported in this mode	Not supported in this mode
	10	7 and 8			
	11	6 and 9			
Rev 2.1 6-channel (01)	00 or 01	3 and 4	Not supported in this mode	7 and 8	6 and 9
	10	7 and 8		3 and 4	6 and 9
	11	6 and 9		7 and 8	3 and 4
Quad (10)	00 or 01	3 and 4	7 and 8	7 and 8	6 and 9
	10	7 and 8	3 and 4	3 and 4	6 and 9
	11	6 and 9	7 and 8	7 and 8	3 and 4

Table 8 Slot to DAC and I2S Mapping Based on Mode and Codec ID

SLAVE CODEC REGISTER ACCESS DEFINITIONS

Master Codec access is exactly as defined for AC'97. For slave Codec access, the AC'97 Digital Controller must invalidate the tag bits for Slot 1 and 2 Command Address and Data (Slot 0, bits 14 and 13) and place a non-zero value (01, 10, or 11) into the Codec ID field (Slot 0, bits 1 and 0).

Slave Codecs disregard the Command Address and Command Data (Slot 0, bits 14 and 13) tag bits when they see a 2-bit Codec ID value (Slot 0, bits 1 and 0) that matches their configuration. In a sense the Slave Codec ID field functions as an alternative Valid Command Address (for Slave reads and writes) and Command Data (for Slave writes) tag indicator.

Slave Codecs must monitor the Frame Valid bit, and ignore the frame (regardless of the state of the Slave Codec ID bits) if it is not valid. AC'97 Digital Controllers should set the frame valid bit for a frame with a slave register access, even if no other bits in the output tag slot except the Slave Codec ID bits are set.

OUTPUT TAG SLOT (16-BITS)	
BIT	**DESCRIPTION**
15	Frame Valid
14	Slot 1 Valid Command Address Bit (Master Codec only)
13	Slot 2 Valid Command Data Bit (Master Codec only)
12-3	Slot 3-12 Valid Bits as defined by AC'97
2	Reserved (Set to 0)
1-0	2-bit Codec ID field (00 reserved for Master; 01, 10, 11 indicate Slave)
New definitions for Slave Codec Register Access	

Table 9 Slave Codec Register Access Slot 0-Bit Definitions

CONTROL INTERFACE

A digital interface has been provided to control the WM9704Q and transfer data to and from it. This serial interface is compatible with the Intel AC'97 specification as illustrated in Figure 7.

The main control interface functions are:

- Control of analogue gain and signal paths through the mixer.
- Bi-directional transfer of ADC and DAC words to and from AC'97 controller.
- Selection of powerdown modes.

AC-LINK DIGITAL SERIAL INTERFACE PROTOCOL

The WM9704Q incorporates a 5-pin digital serial interface that links it to the AC'97 controller. AC-link is a bi-directional, fixed rate, serial PCM digital stream. It handles multiple input and output audio streams, as well as control register accesses employing a time division multiplexed (TDM) scheme. The AC-link architecture divides each audio frame into 12 outgoing and 12 incoming data streams, each with 20-bit sample resolution. With a minimum required DAC and ADC resolution of 16-bits, AC'97 may also be implemented with 18 or 20-bit DAC/ADC resolution, given the headroom that the AC-link architecture provides. The WM9704Q provides support for 18-bit operation.

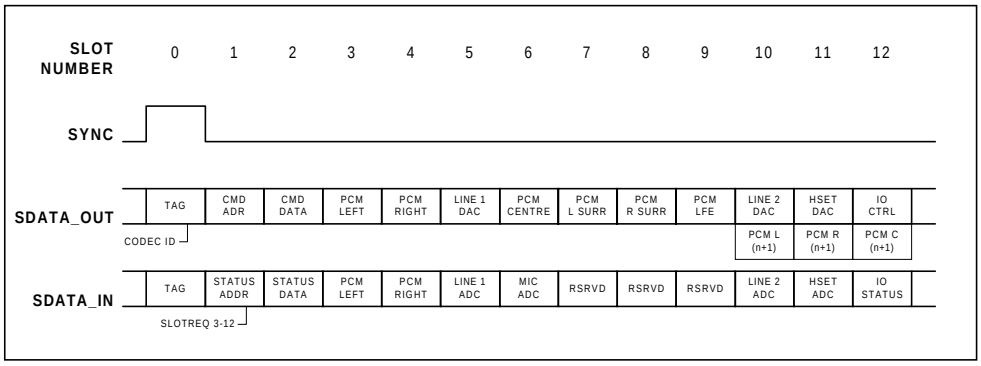


Figure 8 AC'97 Standard Bi-directional Audio Frame

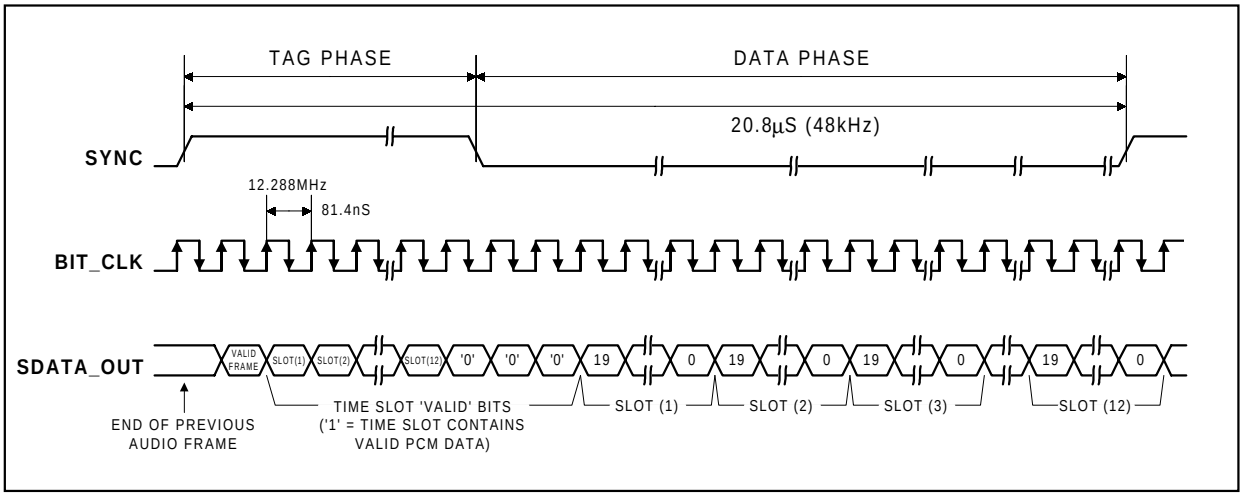


Figure 9 AC-link Audio Output Frame

The datastreams currently defined by the AC'97 specification include:

PCM playback - 2 output slots	2-channel composite PCM output stream
PCM record data - 2 input slots	2-channel composite PCM input stream
Control - 2 output slots	Control register write port
Status - 2 input slots	Control register read port
Optional dedicated microphone input - 1 input slot	Dedicated microphone input stream in support of stereo AEC and/or other voice applications.

Synchronisation of all AC-link data transactions is signalled by the WM9704Q controller. The WM9704Q drives the serial bit clock onto AC-link, which the AC'97 controller then qualifies with a synchronisation signal to construct audio frames.

SYNC, fixed at 48kHz, is derived by dividing down the serial clock (BIT_CLK). BIT_CLK, fixed at 12.288MHz, provides the necessary clocking granularity to support 12, 20-bit outgoing and incoming time slots. AC-link serial data is transitioned on each rising edge of BIT_CLK. The receiver of AC-link data, (WM9704Q for outgoing data and AC'97 controller for incoming data), samples each serial bit on the falling edges of BIT_CLK.

The AC-link protocol provides for a special 16-bit time slot (slot 0) wherein each bit conveys a valid tag for its corresponding time slot within the current audio frame. A 1 in a given bit position of slot 0 indicates that the corresponding time slot within the current audio frame has been assigned to a data stream, and contains valid data. If a slot is tagged invalid, it is the responsibility of the source of the data, (the WM9704Q for the input stream, AC'97 controller for the output stream), to stuff all bit positions with 0s during that slot's active time.

SYNC remains high for a total duration of 16 BIT_CLKs at the beginning of each audio frame.

The portion of the audio frame where SYNC is high is defined as the Tag Phase. The remainder of the audio frame where SYNC is low is defined as the Data Phase. Additionally, for power savings, all clock, sync, and data signals can be halted. This requires that the WM9704Q be implemented as a static design to allow its register contents to remain intact when entering a power savings mode.

AC-LINK AUDIO OUTPUT FRAME (SDATA_OUT)

The audio output frame data streams correspond to the multiplexed bundles of all digital output data targeting the WM9704Q's DAC inputs, and control registers. As briefly mentioned earlier, each audio output frame supports up to 12 20-bit outgoing data time slots. Slot 0 is a special reserved time slot containing 16-bits, which are used for AC-link protocol infrastructure.

Within slot 0 the first bit is a global bit (SDATA_OUT slot 0, bit 15) which flags the validity for the entire audio frame. If the Valid Frame bit is a 1, this indicates that the current audio frame contains at least one time slot of valid data. The next 12-bit positions sampled by the WM9704Q indicate which of the corresponding 12 time slots contain valid data.

In this way data streams of differing sample rates can be transmitted across AC-link at its fixed 48kHz audio frame rate. Figure 9 illustrates the time slot based AC-link protocol.

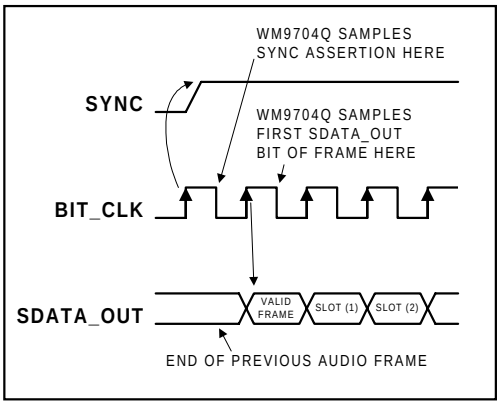


Figure 10 Start of an Audio Output Frame

A new audio output frame begins with a low to high transition of SYNC as shown in Figure 10. SYNC is synchronous to the rising edge of BIT_CLK. On the immediately following falling edge of BIT_CLK, the WM9704Q samples the assertion of SYNC. This falling edge marks the time when both sides of AC-link are aware of the start of a new audio frame. On the next rising edge of BIT_CLK, AC'97 transitions SDATA_OUT into the first bit position of slot 0 (Valid Frame bit). Each new bit position is presented to AC-link on a rising edge of BIT_CLK, and subsequently sampled by the WM9704Q on the following falling edge of BIT_CLK. This sequence ensures that data transitions and subsequent sample points for both incoming and outgoing data streams are time aligned.

Baseline AC'97 specified audio functionality MUST ALWAYS sample rate convert to and from a fixed 48ks/s on the AC'97 controller. This requirement is necessary to ensure that interoperability between the AC'97 controller and the WM9704Q, among other things, can be guaranteed by definition for baseline specified AC'97 features.

SDATA_OUT's composite stream is MSB justified (MSB first) with all non-valid slot bit positions stuffed with 0s by the AC'97 controller. In the event that there are less than 20 valid bits within an assigned and valid time slot, the AC'97 controller always stuffs all trailing non-valid bit positions of the 20-bit slot with 0s.

As an example, consider an 8-bit sample stream that is being played out to one of the WM9704Q's DACs. The first 8 bit positions are presented to the DAC (MSB justified) followed by the next 12 bit positions, which are stuffed with 0s by the AC'97 controller. This ensures that regardless of the resolution of the implemented DAC (16, 18 or 20-bit), no DC biasing will be introduced by the least significant bits. When mono audio sample streams are output from the AC'97 controller, it is necessary that BOTH left and right sample stream time slots be filled with the same data.

SLOT 1: COMMAND ADDRESS PORT

The command port is used to control features and monitor status for the WM9704Q functions including, but not limited to, mixer settings, and power management (refer to the register section). The control interface architecture supports up to 64, 16-bit read/write registers, addressable on even byte boundaries. Only the even registers (00h, 02h, etc.) are valid, odd register (01h, 03h, etc.) accesses are discouraged (if supported they should default to the preceding even byte boundary - i.e. a read to 01h will return the 16-bit contents of 00h). The WM9704Q's control register file is nonetheless readable as well as writeable to provide more robust testability.

Audio output frame slot 1 communicates control register address, and read/write command information to the WM9704Q.

COMMAND ADDRESS PORT BIT ASSIGNMENTS

Bit (19)	Read/write command (1 = read, 0 = write)
Bit (18:12)	Control register index (64 16-bit locations, addressed on even byte boundaries)
Bit (11:0)	Reserved (stuffed with 0s)

The first bit (MSB) sampled by the WM9704Q indicates whether the current control transaction is a read or write operation. The following 7 bit positions communicate the targeted control register address. The trailing 12 bit positions within the slot are reserved and must be stuffed with 0s by the AC'97 controller.

SLOT 2: COMMAND DATA PORT

The command data port is used to deliver 16-bit control register write data in the event that the current command port operation is a write cycle. (As indicated by slot 1, bit 19).

Bit (19:4)	Control register write data (stuffed with 0s if current operation is a read)
Bit (3:0)	Reserved (stuffed with 0s)

If the current command port operation is a read then the entire time slot must be stuffed with 0s by the AC'97 controller.

SLOT 3: PCM PLAYBACK LEFT CHANNEL

Audio output frame slot 3 is the composite digital audio left playback stream. In a typical Games Compatible PC this slot is composed of standard PCM (.wav) output samples digitally mixed (on the AC'97 controller or host processor) with music synthesis output samples. If a sample stream of resolution less than 20-bits is transferred, the AC'97 controller must stuff all trailing non-valid bit positions within this time slot with 0s.

SLOT 4: PCM PLAYBACK RIGHT CHANNEL

Audio output frame slot 4 is the composite digital audio right playback stream. In a typical Games Compatible PC this slot is composed of standard PCM (.wav) output samples digitally mixed (on the AC'97 controller or host processor) with music synthesis output samples.

If a sample stream of resolution less than 20-bits is transferred, the AC'97 controller must stuff all trailing non-valid bit positions within this time slot with 0s.

SLOT 5: OPTIONAL MODEM LINE 1 CODEC

Slot 5 is not supported.

SLOTS 6 TO 9: SURROUND SOUND DATA

Audio output frame slots 6 to 9 are used to send surround sound data to the extra DAC channels. These slots are supported by WM9704Q in Revision 2.1 6-channel mode and Quad mode. Note that the data in the surround sound slots may be applied to either the internal DACs, or sent out onto the GPIO pins as I^2S data, depending upon the mode and ID that has been selected.

SLOT 10: OPTIONAL MODEM LINE2 CODEC

Slot 10 is not supported.

SLOT 11: HANDSET DAC

Slot 11 is not supported.

SLOT 12: GPIO CONTROL

Data in this slot is applied to the GPIO pins, if they have been enabled via the control registers. Note that only bits 11, 12 and 13 are supported, all others are ignored.

AC-LINK AUDIO INPUT FRAME (SDATA_IN)

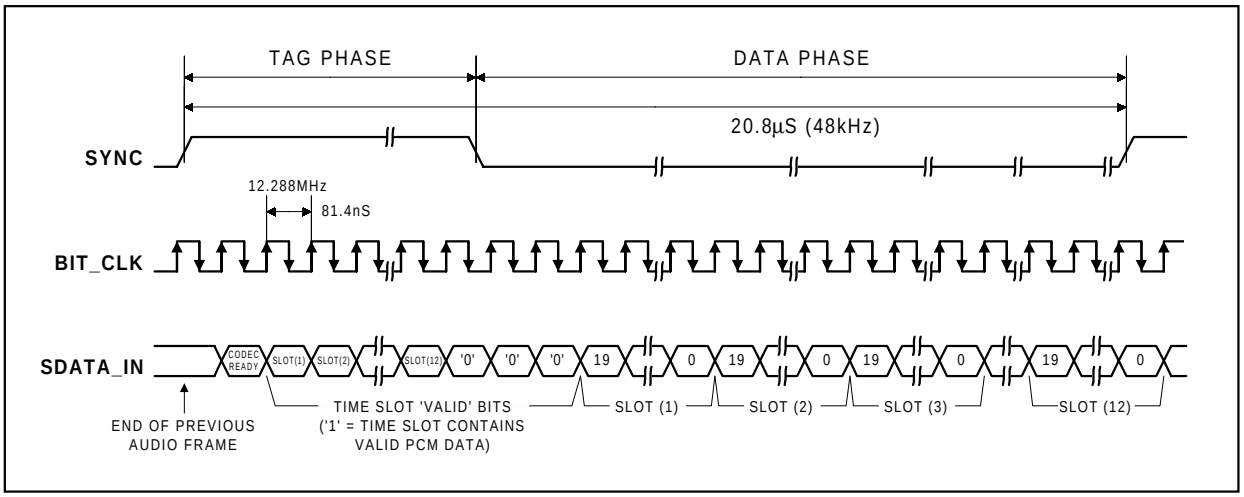


Figure 11 AC-link Audio Input Frame

The audio input frame data streams correspond to the multiplexed bundles of all digital input data targeting the AC'97 controller. As is the case for audio output frame, each AC-link audio input frame consists of 12, 20-bit time slots.

Slot 0 is a special reserved time slot containing 16-bits, which are used for AC-link protocol infrastructure.

Within slot 0 the first bit is a global bit (SDATA_IN slot 0, bit 15) which flags whether the WM9704Q is in the Codec Ready state or not. If the Codec Ready bit is a 0, this indicates that the WM9704Q is not ready for normal operation. This condition is normal following the desertion of power on reset for example, while the WM9704Q's voltage references settle. When the AC-link Codec Ready indicator bit is a 1, it indicates that the AC-link and the WM9704Q control and status registers are in a fully operational state. The AC'97 controller must further probe the Powerdown Control/Status Register to determine exactly which subsections, if any, are ready.

Prior to any attempts at putting the WM9704Q into operation the AC'97 controller should poll the first bit in the audio input frame (SDATA_IN slot 0, bit 15) for an indication that the WM9704Q has gone Codec Ready.

Once the WM9704Q is sampled Codec Ready then the next 12 bit positions sampled by the AC'97 controller indicate which of the corresponding 12 time slots are assigned to input data streams, and that they contain valid data. Figure 11 illustrates the time slot based AC-link protocol.

There are several subsections within the WM9704Q that can independently go busy/ready. It is the responsibility of the WM9704Q controller to probe more deeply into the WM9704Q register file to determine which the WM9704Q subsections are actually ready.

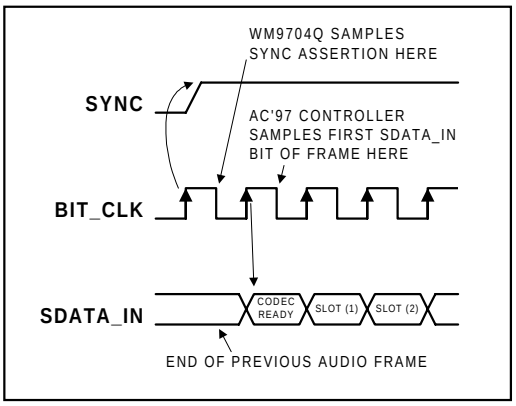


Figure 12 Start of an Audio Input Frame

A new audio input frame begins with a low to high transition of SYNC as shown in Figure 12. SYNC is synchronous to the rising edge of BIT_CLK. On the immediately following falling edge of BIT_CLK, the WM9704Q samples the assertion of SYNC. This falling edge marks the time when both sides of AC-link are aware of the start of a new audio frame. On the next rising edge of BIT_CLK, the AC'97 controller transitions SDATA_IN into the first bit position of slot 0 (valid frame bit). Each new bit position is presented to AC-link on a rising edge of BIT_CLK, and subsequently sampled by the AC'97 controller on the following falling edge of BIT_CLK. This sequence ensures that data transitions and subsequent sample points for both incoming and outgoing data streams are time aligned.

SDATA_IN's composite stream is MSB justified (MSB first) with all non-valid bit positions (for assigned and/or unassigned time slots) stuffed with 0s by the WM9704Q. SDATA_IN is sampled on the falling edges of BIT_CLK.

SLOT 1: STATUS ADDRESS PORT

The status port is used to monitor status for the WM9704Q functions including, but not limited to, mixer settings, and power management.

Audio input frame slot 1 echoes the control register index, for historical reference, for the data to be returned in slot 2. (Assuming that slots 1 and 2 had been tagged valid by the WM9704Q during slot 0).

STATUS ADDRESS PORT BIT ASSIGNMENTS*:*

Bit (19)	RESERVED (stuffed with 0s)
Bit (18:12)	Control register index (echo of register index for which data is being returned)
Bit (11:2)	Variable sample rate SLOTREQ bits.
Bit (1:0)	RESERVED (stuffed with 0s)

The first bit (MSB) generated by the WM9704Q is always stuffed with a 0. The following 7-bit positions communicate the associated control register address. The next 10 bits support the AC'97 Rev 2.1 variable sample rate signalling protocol, and the trailing 2 bit positions are stuffed with 0s by AC'97.

SLOT 2: STATUS DATA PORT

The status data port delivers 16-bit control register read data.

Bit (19:4)	Control register read data (stuffed with 0s if tagged invalid by WM9701)
Bit (3:0)	RESERVED (stuffed with 0s)

If slot 2 is tagged invalid by the WM9704Q, then the entire slot will be stuffed with 0s by the WM9704Q.

SLOT 3: PCM RECORD LEFT CHANNEL

Audio input frame slot 3 is the left channel output of the WM9704Q's input Mux, post-ADC.

The WM9704Q's ADCs can be implemented to support 16, 18, or 20-bit resolution. The WM9704Q ships out its ADC output data (MSB first), and stuffs any trailing non-valid bit positions with 0s to fill out its 20-bit time slot.

SLOT 4: PCM RECORD RIGHT CHANNEL

Audio input frame slot 4 is the right channel output of the WM9704Q's input Mux, post-ADC.

The WM9704Q's ADCs can be implemented to support 16, 18, or 20-bit resolution.

The WM9704Q ships out its ADC output data (MSB first), and stuffs any trailing non-valid bit positions with 0s to fill out its 20-bit time slot.

SLOT 5: OPTIONAL MODEM LINE 1 CODEC

Slot 5 is not supported.

SLOT 10: OPTIONAL MODEM LINE 2 CODEC

Slot 10 is not supported.

SLOT 6: OPTIONAL DEDICATED MICROPHONE RECORD DATA

Audio input frame slot 6 is an optional (post-ADC) third PCM system, input channel available for dedicated use by a desktop microphone. This optional AC'97 feature is not supported by the WM9704Q. This may be determined by the AC'97 controller interrogating the WM9704Q Vendor ID register.

SLOTS 7 TO 11: RESERVED

Audio input frame slots 7 to 11 are reserved for future use and are always stuffed with 0s by AC '97.

SLOT 12:

GPIO functions supported.

AC-LINK LOW POWER MODE

The AC-link signals can be placed in a low power mode. When the WM9704Q's powerdown Register 26h, is programmed to the appropriate value, both BIT_CLK and SDATA_IN will be brought to, and held at a logic low voltage level.

BIT_CLK and SDATA_IN are transitioned low immediately following the decode of the write to the Powerdown Register (26h) with PR4. When the AC'97 controller driver is at the point where it is ready to program the AC-link into its low power mode, slots 1 and 2 are assumed to be the only valid stream in the audio output frame. At this point in time it is assumed that all sources of audio input have also been neutralised.

The AC'97 controller should also drive SYNC and SDATA_OUT low after programming the WM9704Q to this low power, halted mode.

Once the WM9704Q has been instructed to halt BIT_CLK, a special wake up protocol must be used to bring the AC-link to the active mode since normal audio output and input frames can not be communicated in the absence of BIT_CLK.

WAKING UP THE AC-LINK

There are 2 methods for bringing the AC-link out of a low power, halted mode. Regardless of the method, it is the AC'97 controller that performs the wake up task.

AC-link protocol provides for a Cold WM9704Q Reset, and a Warm WM9704Q Reset.

The current powerdown state would ultimately dictate which form of WM9704Q reset is appropriate. Unless a cold or register reset (a write to the reset register) is performed, wherein the WM9704Q registers are initialised to their default values, registers are required to keep state during all powerdown modes.

Once powered down, re-activation of the AC-link via re-assertion of the SYNC signal must not occur for a minimum of 4 audio frame times following the frame in which the powerdown was triggered. When AC-link powers up it indicates readiness via the Codec Ready bit (input slot 0, bit 15).

COLD WM9704Q RESET

A cold reset is achieved by asserting RESETB for the minimum specified time. By driving RESETB low, BIT_CLK, and SDATA_OUT will be activated, or re-activated as the case may be, and all the WM9704Q control registers will be initialised to their default power on reset values.

RESETB is an asynchronous WM9704Q input.

WARM WM9704Q RESET

A warm WM9704Q reset will re-activate the AC-link without altering the current WM9704Q register values. A warm reset is signalled by driving SYNC high for a minimum of 1µS in the absence of BIT_CLK.

Within normal audio frames SYNC is a synchronous the WM9704Q input. However, in the absence of BIT_CLK, SYNC is treated as an asynchronous input used in the generation of a warm reset to the WM9704Q. The WM9704Q will not respond with the activation of BIT_CLK until SYNC has been sampled low again by the WM9704Q. This will preclude the false detection of a new audio frame.

SERIAL INTERFACE REGISTER MAP DESCRIPTION

(See Table 24)

The serial interface bits perform control functions described as follows. Note that the register map is fully specified by the AC'97 specification, and this description is simply repeated below, with optional unsupported features omitted.

RESET REGISTER (INDEX 00h)

Writing any value to this register performs a register reset, which causes all registers to revert to their default values. Reading this register returns the ID code of the part, indication of modem support (not supported by the WM9704Q) and a code for the type of 3D stereo enhancement.

BIT	FUNCTION	VALUE ON WM9704Q
ID0	Dedicated Mic PCM in channel	0
ID1	Modem line Codec support	0
ID2	Bass and treble control	0
ID3	Simulated stereo (mono to stereo)	0
ID4	Headphone out support	0
ID5	Loudness (bass boost) support	0
ID6	18-bit DAC resolution	1
ID7	20-bit DAC resolution	0
ID8	18-bit ADC resolution	1
ID9	20-bit ADC resolution	0
SE4...SE0	3D stereo enhancement technique	11000

Table 10 Reset Register Function

Note that the WM9704Q defaults to indicate 18-bit compatibility. However, a control bit may be set in the vendor-specific registers that changes bits ID6 and ID8 to be 0, indicating a 16-bit device. It is unlikely that this function will be required, however, as the MSB justification of the ADC and DAC data means that a nominally 18-bit device should be fully compatible with controllers that only provide 16-bit support. Most PC type applications will only require 16-bit operation.

PLAY MASTER VOLUME REGISTERS (INDEX 02h, 04h AND 06h)

These registers manage the output signal volumes. Register 02h controls the stereo master volume (both right and left channels), Register 04h controls the optional stereo headphone out, and Register 06h controls the mono volume output. Each step corresponds to 1.5dB. The MSB of the register is the mute bit. When this bit is set to 1 the level for that channel is set at -∞dB.

ML5 through ML0 is for left channel level, ML5 through ML0 is for the right channel and MM5 through MM0 is for the mono out channel.

Support for the MSB of the volume level is not provided by the WM9704Q. If the MSB is written to, then the WM9704Q detects when that bit is set and sets all 4 LSBs to 1s. Example: If the driver writes a 1xxxxx the WM9704Q interprets that as x11111. It will also respond when read with x11111 rather than 1xxxxx, the value written to it. The driver can use this feature to detect if support for the 6th bit is there or not.

The default value of both the mono and the stereo registers is 8000h (1000 0000 0000 0000), which corresponds to 0dB gain with mute on.

MUTE	MX4...MX0	FUNCTION
0	0 0000	0dB attenuation
0	0 0001	1.5dB attenuation
0	1 1111	46.5dB attenuation
1	x xxxx	∞dB attenuation

Table 11 Volume Register Function

MASTER TONE CONTROL REGISTERS (INDEX 08h)

Optional register for support of tone controls (bass and treble). The WM9704Q does not support bass and treble and writing to this register will have no effect, reading will result in all don't care values.

PC BEEP REGISTER (INDEX 0Ah)

This controls the level for the PC-beep input. Each step corresponds to approximately 3dB of attenuation. The MSB of the register is the mute bit. When this bit is set to 1 the level for that channel is set at -∞dB.

WM9704Q defaults to the PC-beep path being muted, so an external speaker should be provided within the PC to alert the user to power on self-test problems.

MUTE	PV3...PV0	FUNCTION
0	0000	0dB attenuation
0	1111	45dB attenuation
1	xxxx	∞dB attenuation

Table 12 PC-beep Register Function

ANALOGUE MIXER INPUT GAIN REGISTERS (INDEX 0Ch - 18h)

This controls the gain/attenuation for each of the analogue inputs. Each step corresponds to approximately 1.5dB. The MSB of the register is the mute bit. When this bit is set to 1 the level for that channel is set at -∞dB. (See Table 13).

REGISTER 0Eh (MIC VOLUME REGISTER)

This has an extra bit that is for a 20dB boost. When bit 6 is set to 1 the 20dB boost is on. The default value is 8008, which corresponds to 0dB gain with mute on.

The default value for the mono registers is 8008h, which corresponds to 0dB gain with mute on. The default value for stereo registers is 8808h, which corresponds to 0dB gain with mute on.

MUTE	GX4...GX0	FUNCTION
0	00000	+12dB gain
0	01000	0dB gain
0	11111	-34.5dB gain
1	xxxxx	-∞dB gain

Table 13 Mixer Gain Control Register Function

RECORD SELECT CONTROL REGISTER (INDEX 1Ah)

Used to select the record source independently for right and left (see Table 14). The default value is 0000h, which corresponds to Mic in.

SR2 TO SR0	RIGHT RECORD SOURCE	SL2 TO SL0	LEFT RECORD SOURCE
0	Mic	0	Mic
1	CD in (R)	1	CD in (L)
2	Video in (R)	2	Video in (L)
3	Aux in (R)	3	Aux in (L)
4	Line in (R)	4	Line in (L)
5	Stereo mix (R)	5	Stereo mix (L)
6	Mono mix	6	Mono mix
7	Phone	7	Phone

Table 14 Record Select Register Function

RECORD GAIN REGISTERS (INDEX 1Ch AND 1Eh)

1Ch is for the stereo input and 1Eh is for the optional special purpose correlated audio Mic channel. Each step corresponds to 1.5dB. 22.5dB corresponds to 0F0Fh and 000Fh respectively. The MSB of the register is the mute bit. When this bit is set to 1, the level for that channel(s) is set at -∞dB.

The default value is 8000h, which corresponds to 0dB gain with mute on.

MUTE	GX3...GX0	FUNCTION
0	1111	+22.5dB gain
0	0000	0dB gain
1	xxxxx	-∞dB gain

Table 15 Record Gain Register Function

GENERAL PURPOSE REGISTER (INDEX 20h)

This register is used to control several miscellaneous functions of the WM9704Q.

Below is a summary of each bit and its function. Only the MIX, MS and LPBK bits are supported by the WM9704Q. The MS bit controls the Mic selector. The LPBK bit enables loopback of the ADC output to the DAC input without involving the AC-link, allowing for full system performance measurements. The function default value is 0000h, which is all off.

BIT	FUNCTION	WM9704Q SUPPORT
POP	PCM out path and mute, 0 = pre-3D, 1 = post-3D	Yes, but fixed at 1
ST	Simulated stereo enhancement, on/off 1 = on	No
3D	3D stereo enhancement on/off, 1 = on	Yes
LD	Loudness (bass boost) on/off, 1 = on	No
LLBK	Local loop back - for modem, line codec	No
RLBK	Remote loop back - for modem, line codec	No
MIX	Mono output select 0 = Mix, 1 = Mic	Yes
MS	Mic select 0 = Mic1, 1 = Mic2	Yes
LPBK	ADC/DAC/ loopback mode	Yes

Table 16 General Purpose Register Function

3D CONTROL REGISTER (INDEX 22h)

This register is used to control the centre and/or depth of the 3D stereo enhancement function built into of the AC '97 component. Only the depth bits DP0 to 3 have effect in the WM9704Q.

DP3…DP0	DEPTH
0	0%
1	
-	
8	Typical value
-	
15	100%

RESERVED REGISTER (INDEX 24h)

Not supported by the WM9704Q.

POWERDOWN CONTROL/STATUS REGISTER (INDEX 26h)

This read/write register is used to program powerdown states and monitor subsystem readiness. The lower half of this register is read only status, a 1 indicating that the subsection is ready. Ready is defined as the subsection able to perform in its nominal state. When this register is written the bit values that come in on AC-link will have no effect on read only bits 0 to 7.

When the AC-link Codec Ready indicator bit (SDATA_IN slot 0, bit 15) is a 1, it indicates that the AC-link and the WM9704Q control and status registers are in a fully operational state. The AC'97 controller must further probe this Powerdown Control/Status Register to determine exactly which subsections, if any, are ready.

READ BIT	FUNCTION
REF	VREFs up to nominal level
ANL	Analogue mixers, etc ready
DAC	DAC section ready to accept data
ADC	ADC section ready to transmit data

Table 17 Powerdown Status Register Function

The powerdown modes are as follows. The first three bits are to be used individually rather than in combination with each other. The last bit PR3 can be used in combination with PR2 or by itself. PR0 and PR1 control the PCM ADCs and DACs only. PR6 is not supported by the WM9704Q.

WRITE BIT	FUNCTION
PR0	PCM in ADCs and input Mux powerdown
PR1	PCM out DACs powerdown
PR2	Analogue mixer powerdown (VREF still on)
PR3	Analogue mixer powerdown (VREF off)
PR4	Digital interface (AC-link) powerdown (external clock off)
PR5	Internal clock disable
PR6	HP amp powerdown – not supported
EAPD	External amplifier powerdown

Table 18 Powerdown Control Register Function

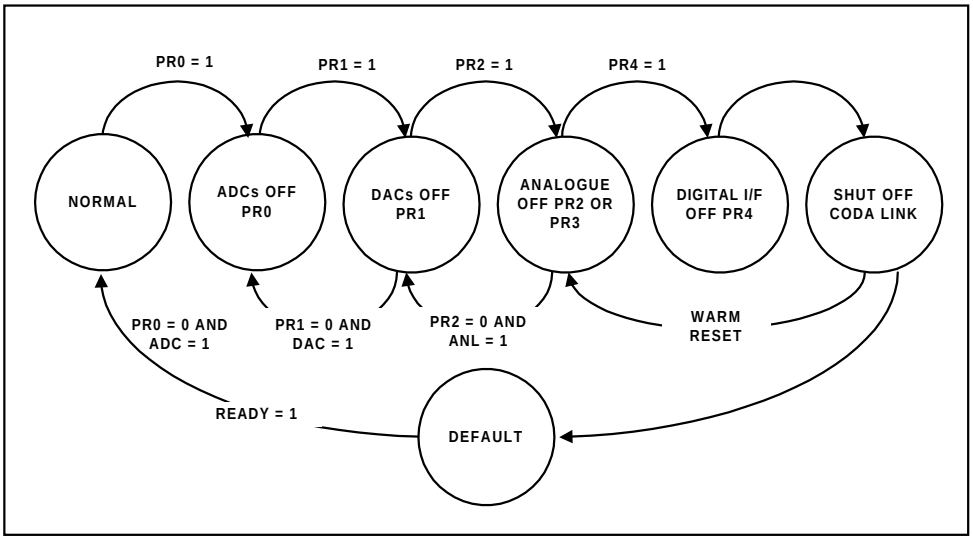


Figure 13 An Example of the WM9704Q Powerdown/Powerup Flow

Figure 13 illustrates one example of a procedure to do a complete powerdown of the WM9704Q. From normal operation sequential writes to the Powerdown Register are performed to powerdown the WM9704Q a piece at a time. After everything has been shut off (PR0 to PR3 set), a final write (of PR4) can be executed to shut down the WM9704Q's digital interface (AC-link).

The part will remain in sleep mode with all its registers holding their static values. To wake up the WM9704Q, the AC'97 controller will send a pulse on the sync line issuing a warm reset. This will restart the WM9704Q's digital interface (resetting PR4 to 0). The WM9704Q can also be woken up with a cold reset. A cold reset will cause a loss of values of the registers, as a cold reset will set them to their default states. When a section is powered back on, the Powerdown Control/Status Register (26h) should be read to verify that the section is ready (i.e. stable) before attempting any operation that requires it.

Alternatively if RESETB is held low, all PR bits are held set so the device is held powered off until RESETB is taken high again.

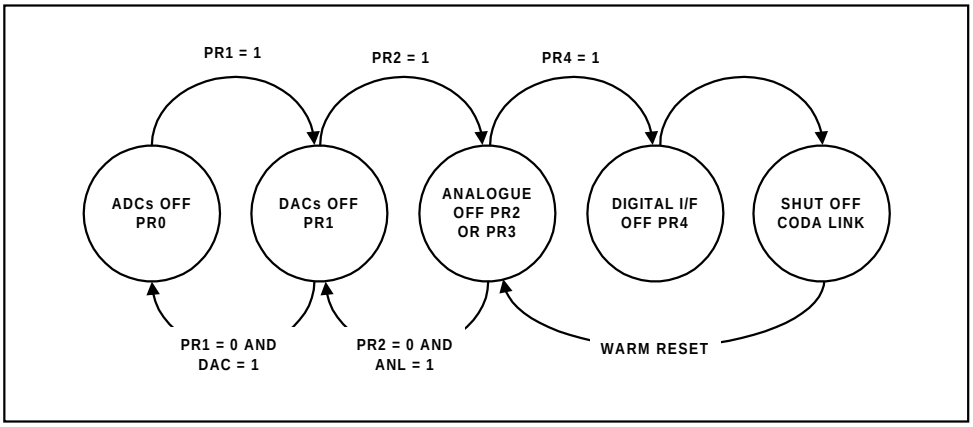


Figure 14 The WM9704Q Powerdown/Flow with Analogue Still Alive

Figure 14 illustrates a state when all the mixers should work with the static volume settings that are contained in their associated registers. This is used when the user is playing a CD (or external LINE_IN source) through WM9704Q to the speakers but has most of the system in low power mode. The procedure for this follows the previous procedure except that the analogue mixer is never shut down.

POWERDOWN CONTROL/STATUS REGISTER (INDEX 26h)

Note that in order to go into ultimate low power mode, PR5 is required to be set which turns off the oscillator circuit. Asserting SYNC resets the PR5 bit and re-starts the oscillator in the same was as the AC link is restarted.

Also when RESETB pin is asserted low, all PR bits are over-ridden and the entire device is powered off to ultra low power state for as long as RESETB = low. On releasing RESETB, the device is reset (all active) and powered up.

VENDOR RESERVED REGISTERS (INDEX 5Ah TO 7Ah)

These are reserved for future use and are vendor specific. Do not write to these registers unless the Vendor ID register has been checked first to ensure that the driver knows the source of the AC'97 component. Values stored in this register are used to provide test modes for the manufacturer

REVISION 2.1 REGISTERS (INDEX 28h T0 58h)

These registers are specified as to use in Revision 2.1 of the AC'97 specification and have the following functions on the WM9704Q:

REGISTER 28h – EXTENDED AUDIO ID

The Extended Audio ID register is a read only register that identifies which extended audio features are supported (in addition to the original AC'97 features identified by reading the reset register at index 00h). A non-zero value indicates the feature is supported. The indication of support for 6-channel surround sound changes depending on whether the WM9704Q is configured in mode 00 or otherwise.

DATA BIT	FUNCTION	ANY MODE BUT 10	MODE 10
VRA	Variable rate audio support	1	1
DRA	Double rate audio support	0	0
VRM	Variable rate Mic ADC support	0	0
CDAC	Centre DAC support	0 (unless I^2S = 1)	1 when ID = 11 or I^2S = 1
SDAC	Surround DAC support	0 (unless I^2S = 1)	1
LDAC	LFE DAC support	0 (unless I^2S = 1)	1 when ID = 11 or I^2S = 1
AMAP	Slot to front DAC mapping support	1	1
ID1	Codec configuration – pin 45 value	Inverse of level at pin 45	Inverse of level at pin 45
ID0	Codec configuration – pin 46 value	Inverse of level at pin 46	Inverse of level at pin 46

Table 19 Extended Audio ID Register

REGISTER 2Ah - EXTENDED AUDIO STATUS AND CONTROL REGISTER

The Extended Audio Status and Control Register is a read/write register that provides status and control of the extended audio features.

DATA BIT	FUNCTION	READ/WRITE	WM9704Q SUPPORT
VRA	Enables variable rate audio mode	Read/write	Yes
DRA	Enable double rate audio mode	Read/write	No
VRM	Enables variable rate Mic ADC	Read/write	No
CDAC	Indicates centre DAC ready	Read	Yes
SDAC	Indicates surround DAC ready	Read	Yes
LDAC	Indicates LFE DAC ready	Read	Yes
MADC	Indicates Mic ADC ready	Read	No
PRI	Set to turn off centre DAC	Read/write	Enable only
PRJ	Set to turn off surround DACs	Read/write	Enable only
PRK	Set to turn off LFE DACs	Read/write	Enable only
PRL	Set to turn off Mic ADC	Read/write	No

Table 20 Extended Audio Status and Control Register

REGISTER 2Ch TO 32h – AUDIO SAMPLE RATE CONTROL REGISTERS

These registers are read/write registers that are written to, to select alternative sample rates for the audio PCM converters. Default is the 48ks/s rate. Note that only Revision 2.1 recommended rates are supported by the WM9704Q, selection of any other unsupported rates will cause the rate to default to the nearest supported rate, and the supported rate value to be latched and so read back.

Register 2Ch is the front DAC rate register, but is also used for centre channel data rate.

I^2S mode ONLY supports 48ks/s rates, NOT variable rates.

REGISTERS 36h AND 38h – 6 CHANNEL VOLUME CONTROL

These read/write registers control the output volume of the optional four PCM channels. Note that as WM9704Q only supports 4 internal DACs, depending upon which ID has been selected via the CID pins 45 and 46, these registers may or may not have effect. The fields behave the same as the master volume control register, which offers attenuation but no gain. If gain is required then the PCM DAC mixer PGAs appropriate to each DAC should be used.

If Quad Mode is selected and ID = 10 or 11, then either 36h or 38h will control the level of the rear DAC outputs onto the line level pins 39 and 41. Surround data which is mapped from the surround data slots out onto the GPIO pins as I^2S data, may not have it's level adjusted. The mute bit will, however, mute the data to all 0s.

GPIO FUNCTION

Note that only the three GPIO pins are supported, GPIO 11 to 13. These pins are available to the user, unless used for I^2S mode. GPIO mode over-rides I^2S function.

REGISTER 4Ch – GPIO PIN CONFIGURATION REGISTER

The GPIO Pin Configuration is a read/write register that specifies whether a GPIO pin is configured for input (1) or for output (0), and is accessed via the standard slot 1 and 2 command address/data protocols.

If a GPIO pin is implemented, the respective GCx bit should be read/writeable and set to 1. If a GPIO is not implemented, then the respective GCx bit is read-only and set to 0. This informs the software how many GPIO pins have been implemented. It is up to the AC'97 Digital Controller to send the desired GPIO pin value over output slot 12 in the outgoing stream of the AC-link before configuring any of these bits for output. The default value after cold or register reset for this register (3800h) is all pins configured as inputs.

REGISTER 4Eh – GPIO PINS POLARITY/TYPE

The GPIO Pin Polarity/Type is a read/write register that defines GPIO input polarity (0 = Low, 1 = High active) when a GPIO pin is configured as an Input. It defines GPIO output type (1 = CMOS, 0 = OPEN-DRAIN) when a GPIO pin is configured as an output.

The default value after cold or register reset for this register (FFFFh) is all pins active high. Non-implemented GPIO pins always return 1s.

REGISTER 50h – GPIO PIN STICKY CONTROL

The GPIO Pin Sticky is a read/write register that defines GPIO Input Type (0 = Non-sticky, 1 = Sticky) when a GPIO pin is configured as an input. GPIO inputs configured as sticky are cleared by writing a 0 to the corresponding bit of the GPIO pin status register 54h (see below), and by reset.

The default value after cold or register reset for this register (0000h) is all pins Non-sticky. Unimplemented GPIO pins always return 0s. Sticky is defined as edge-sensitive, Non-sticky as level sensitive.

REGISTER 52h – GPIO PIN WAKE-UP CONTROL

The GPIO Pin Wake-up is a read/write register that provides a mask for determining if an input GPIO change will generate a wake-up or GPIO_INT (0 = No, 1 = Yes). When the AC-Link is powered down (Register 26h PR4 = 1 for primary codecs), a wake-up event will trigger the assertion of SDATA_IN. When AC-link is powered up, a wake-up event will appear as GPIO_INT = 1 on bit 0 of input slot 12. GPIO_INT is also flagged when the link is active.

An AC-link wake-up interrupt is defined as a 0 to 1 transition on SDATA_IN when the AC-Link is powered down (Register 26h PR4 = 1). GPIO bits that have been programmed as inputs, sticky and pin wake-up, upon transition either (high-to-low) or (low-to-high) depending on pin polarity, will cause an AC-link wake-up event (transition of SDATA_IN from 0 to 1), if and only if the AC-link was powered down.

The default value after cold or register reset for this register (0000h) defaults to all 0s specifying no wake-up event. Non-implemented GPIO pins always return 0s.

REGISTER 54h – GPIO PIN STATUS

The GPIO status is a read/write register that reflects the state of all GPIO pins (inputs and outputs) on slot 12. The value of all GPIO pin inputs and outputs comes in from the codec every frame on slot 12, but is also available for reading as GPIO Pin Status via the standard slot 1 and 2 command address/data protocols. GPIO inputs configured as Sticky are cleared by writing a 0 to the corresponding bit of this register 54h.

Bits corresponding to unimplemented GPIO pins should be forced to zero in this register and input slot 12. GPIO bits that have been programmed as Inputs and Sticky, upon transition either (high-to low) or (low-to-high) depending on pin polarity, will cause the individual GPIO bit to go asserted 1, and remain asserted until a write of 0 to that bit. The normal way to set the desired value of a GPIO output pin is to set the control bit in output slot 12.

The default value, if configured as an input, after cold or register reset for this register is always the state of the GPIO pin.

REGISTER 56h – MISCELLANEOUS MODEM AFE STATUS/CONTROL

Not supported in this mode.

VENDOR RESERVED REGISTERS (INDEX 5Ah AND 7Ah)

These registers are vendor specific. Do not write to these registers unless the Vendor ID register has been checked first to ensure that the driver knows the source of the AC'97 component. Values stored in this register are used to provide vendor specific modes for the manufacturer.

BIT	NAME	DEFAULT	ACTION WHEN SET TO 1
User bits			
AND	ADC no DAC	0	Select stereo mix into ADC as having no DAC signal
R2S	Rev 2.1 switch	0	Closes Rev 2.1 switch when set (see fig 1)
I^2S	I^2S enable	0	Enables I^2S data and clock onto GPIO pins 43,44,48
DLM	Dual line modem	0	Selects support for Line2 DAC and ADC slots
AMD	Automute disable	0	Disables automute function on the front and rear DACs

Table 22 Vendor Register 5Ah Bit Allocation and Default States

VENDOR SPECIFIC GAIN CONTROL REGISTERS – (INDEX 70h TO 74h)

These three registers control the gain and mute functions applied to the front and rear mixer paths, and the rear channel DAC gains. These PGAs are not accommodated in the Intel specification, but are required in order to build a flexible quad surround sound device. The function is as per the other mixer PGAs. However, the default value of the register changes depending upon the MODE the device is operating in, as shown in Table 23.

MODE	DEFAULT VALUE FOR REGISTER			
	REAR DAC – REG 70H	FRONT MIXER – REG 72H	REAR MIXER – REG 74H	REV 2.1 SWITCH
Rev 2.1 (00)	8808	0808	8808	Closed
Rev 2.1 6-channel (01)	8808	0808	8808	Closed
Quad (10)	8808	0808	0808	Open

Table 23 Vendor Specific PGA Default Values

VENDOR ID REGISTERS (INDEX 7Ch TO 7Eh)

This register is for specific vendor identification if so desired. The ID method is Microsoft's Plug and Play Vendor ID code. The first character of that ID is F7 to F0, the second character S7 to S0, and the third T7 to T0. These three characters are ASCII encoded. The REV7 to REV0 field is for the Vendor Revision number. In WM9704Q the vendor ID is set to WML3 if MODE1 = 0, and WML4 if MODE1 = 1.

Wolfson is a registered Microsoft Plug and Play vendor.

SERIAL INTERFACE REGISTER MAP

The following table shows the function and address of the various control bits that are loaded through the serial interface during write operations.

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
00h	Reset	X	SE4	SE3	SE2	SE1	SE0	ID9	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	6150h
02h	Master volume	Mute	X	X	ML4	ML3	ML2	ML1	ML0	X	X	X	MR4	MR3	MR2	MR1	MR0	8000h
04h	Headphone vol.	Mute	X	X	ML4	ML3	ML2	ML1	ML0	X	X	X	MR4	MR3	MR2	MR1	MR0	8000h
06h	Master vol. mono	Mute	X	X	X	X	X	X	X	X	X	X	MM4	MM3	MM2	MM1	MM0	8000h
0Ah	PCBEEP vol.	Mute	X	X	X	X	X	X	X	X	X	X	PV3	PV2	PV2	PV0	X	8000h
0Ch	Phone volume	Mute	X	X	X	X	X	X	X	X	X	X	GN4	GN3	GN2	GN1	GN0	8008h
0Eh	Mic volume	Mute	X	X	X	X	X	X	X	X	20dB	X	GN4	GN3	GN2	GN1	GN0	8008h
10h	Line in volume	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	X	X	GR4	GR3	GR2	GR1	GR0	8808h
12h	CD volume	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	X	X	GR4	GR3	GR2	GR1	GR0	8808h
14h	Video volume	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	X	X	GR4	GR3	GR2	GR1	GR0	8808h
16h	Aux volume	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	X	X	GR4	GR3	GR2	GR1	GR0	8808h
18h	Frnt PCM out volume	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	X	X	GR4	GR3	GR2	GR1	GR0	8808h
1Ah	Rec. select	X	X	X	X	X	SL2	SL1	SL0	X	X	X	X	X	SR2	SR1	SR0	0000h
1Ch	Rec. gain	Mute	X	X	X	GL3	GL2	GL1	GL0	X	X	X	X	GR3	GR2	GR1	GR0	8000h
20h	General purpose	POP	ST	3D	ID	X	X	MIX	MS	LPBK	X	X	X	X	X	X	X	8000h
22h	3D control	X	X	X	X	X	X	X	X	X	X	X	X	DP3	DP2	DP1	DP0	0000h
24h	Reserved	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0000h
26h	Pwrdwn ctrl/stat	EAPD	PR6	PR5	PR4	PR3	PR2	PR1	PR0	X	X	X	X	REF	ANL	DAC	ADC	000Fh
28h	Ext'd audio ID	ID1	ID0	X	X	X	X	Amap	Ldac	Sdac	Cdac	X	X	VRM	X	DRA	VRA	0281h
2Ah	Ext'd audio ctrl/stat	X	PRL	PRK	PRJ	PRI	X	Madc	Ldac	Sdac	Cdac	X	X	VRM	X	DRA	VRA	0080h
2Ch	Front DAC rate	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h
2Eh	Rear DAC rate	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h
30h	LFE DAC rate	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h
32h	Audio ADC rate	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h
36h	6ch vol. C,LFE	Mute	X	X	LFE4	LFE3	LFE2	LFE1	LFE0	Mute	X	X	CNT4	CNT3	CNT2	CNT1	CNT 0	8080h
38h	6ch vol. L,R surr	Mute	X	X	LSR4	LSR3	LSR2	LSR1	LSR0	Mute	X	X	RSR4	RSR3	RSR2	RSR1	RSR0	8080h
3Ch	Ext'd mdm ID	ID1	ID0	X	X	X	X	X	X	X	X	X	CID2	CID1	HSET	LIN2	LIN1	x00xh
3Eh	Ext'd mdm stat	PRH	PRG	PRF	PRE	PD	PRC	PRB	PRA	HDAC	HADC	DAC2	ADC2	DAC1	ADC1	MREF	GPIO	0100h
40h	Line1 sample rate ADC/DAC	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h
42h	Line2 sample rate ADC/DAC	Sample rates written to 42h will alias onto 40h																
46h	Line1 DAC/ADC level	Not supported - set TX modem levels by writing to rear DAC PGA 04h																
48h	Line2 DAC/ADC level	Not supported - set TX modem levels by writing to rear DAC PGA 04h																
4Ch	GPIO pin config	0	0	GW13	GW12	GW1	0	0	0	0	0	0	0	0	0	0	0	000Eh
4Eh	GPIO pin type	1	1	GC13	GC12	GC11	1	1	1	1	1	1	1	1	1	1	1	FFFFh
50h	GPIO pin sticky	0	0	GP13	GP12	GP11	0	0	0	0	0	0	0	0	0	0	0	0000h
52h	GPIO wake-up	0	0	GS13	GS12	GS11	0	0	0	0	0	0	0	0	0	0	0	0000h
54h	GPIO pin status	0	0	GI13	GI12	GI11	0	0	0	0	0	0	0	0	0	0	0	000xh
56h	Misc. modem ctrl/stat	CID2	CID1	CIDR	MLNK	X	HSB2	HSB1	HSB0	X	L2B2	L2B1	L2B0	X	L1B2	L1B1	L1B 0	0000h
5Ah	Vendor rsvd test	ATST	DTST	AFTS	DFTS	RTST	DDS	AMD	DLM	I2S	R2S	AND	HIM	HIC	TRM	BB	AEV	0000h
70h	Rr PCM out vol.	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	X	X	GR4	GR3	GR2	GR1	GR0	0808h
72h	Front mixer vol.	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	X	X	GR4	GR3	GR2	GR1	GR0	8808h
74h	Rear mixer vol.	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	X	X	GR4	GR3	GR2	GR1	GR0	8808h
7Ah	Vendor rsvd	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
7Ch	Vendor ID1	F7	F6	F5	F4	F3	F2	F1	F0	S7	S6	S5	S4	S3	S2	S1	S0	574Dh
7Eh	Vendor ID2	T7	T6	T5	T4	T3	T2	T1	T0	Rev7	Rev6	Rev5	Rev4	Rev3	Rev2	Rev1	Rev 0	4C0xh

Table 24 Serial Interface Register Map Description

RECOMMENDED EXTERNAL COMPONENTS

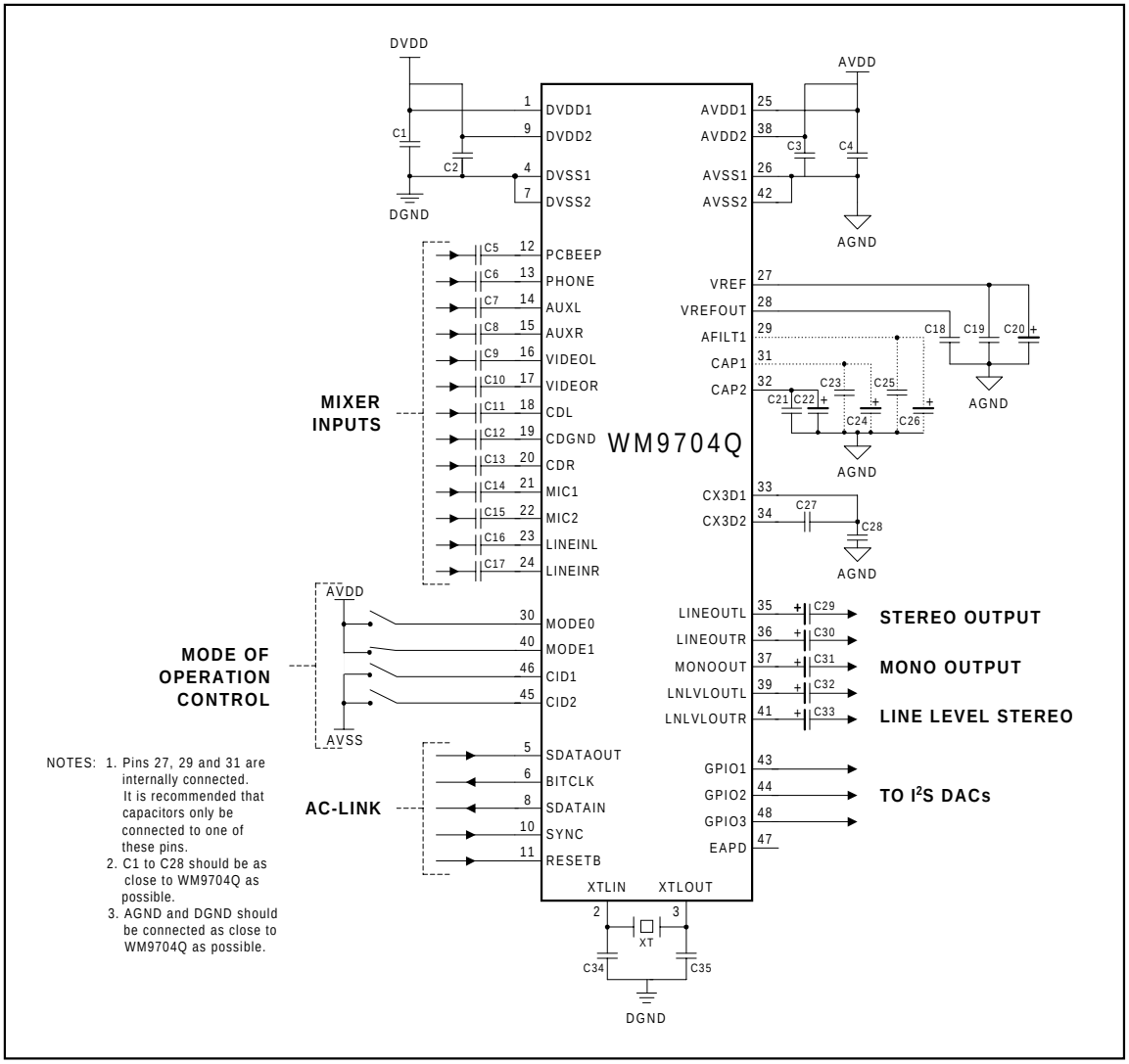


Figure 15 External Components Diagram

RECOMMENDED EXTERNAL COMPONENTS VALUES

COMPONENT REFERENCE	SUGGESTED VALUE	DESCRIPTION
C1 to C4	10nF	De-coupling for DVDD and AVDD
C5 to C17	470nF	AC coupling capacitors for setting DC level of analogue inputs to VCAP1. Value chosen to give corner frequency below 20Hz for min 10K input impedance.
C18	1µF	Reference de-coupling capacitors for ADC, DAC, Mixer and CAP2 references. Ceramic type or similar.
C19	0.1µF	
C20	10µF	
C21	0.1µF	
C22	10µF	
C23	0.1µF	
C24	10µF	
C25	0.1µF	
C26	10µF	
C27	100nF	3D low pass filter. This value sets nominal 100Hz.
C28	47nF	3D high pass filter. This value sets nominal 1kHz.
C29 to C33	10µF	Output AC coupling caps to remove VREF DC level from outputs.
C34 and C35	22pF	Optional capacitors for better crystal frequency stability.
XT	24.576 MHz	AC'97 master clock frequency. A bias resistor is not required, but if connected will not affect operation if value is large (above 1MΩ).

Table 25 External Component Values

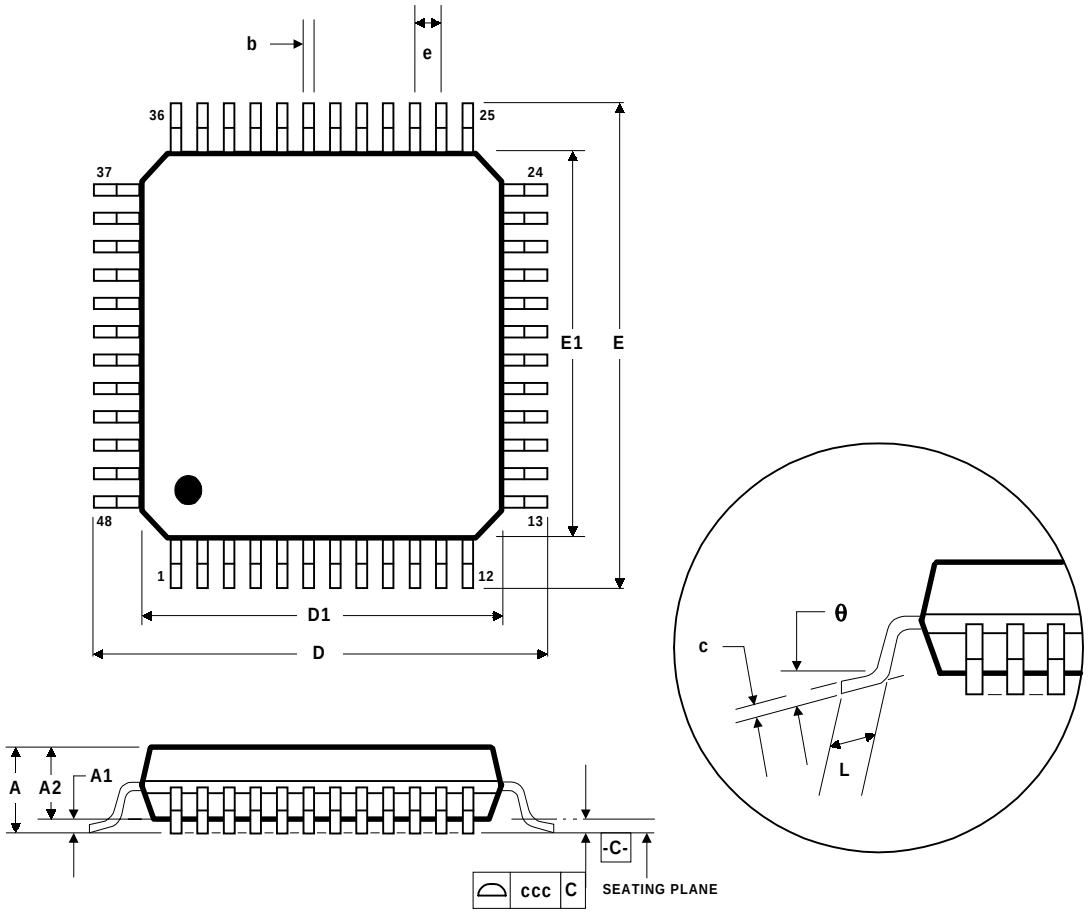
RECOMMENDATIONS FOR 3.3V OPERATION

The device's performance with AVDD = 3.3V is shown in Electrical Characteristics.

In 3.3V analogue operation, mid-rail reference scales to 1.5V. All ADC and DAC references are 3/5^{ths} of their nominal 5V value. Input and output signals that are 1Vrms in 5V applications, scale to 660mVrms in 3.3V applications. If 1Vrms output is required, the mixer gain adjust PGAs need to be increased by 3 times 1.5dB steps.

PACKAGE DIMENSIONS

FT: 48 PIN TQFP (7 x 7 x 1.4 mm) **DM003.B**



Symbols	Dimensions (mm)		
	MIN	NOM	MAX
A	-----	-----	1.60
A_1	0.05	-----	0.15
A_2	1.35	1.40	1.45
b	0.17	0.22	0.27
c	0.09	-----	0.20
D	9.00 BSC		
D_1	7.00 BSC		
E	9.00 BSC		
E_1	7.00 BSC		
e	0.50 BSC		
L	0.45	0.60	0.75
θ	0^o	3.5^o	7^o
Tolerances of Form and Position			
ccc	0.08		
REF:	JEDEC.95, MS-026		

NOTES:
A. ALL LINEAR DIMENSIONS ARE IN MILLIMETERS.
B. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.
C. BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSION, NOT TO EXCEED 0.25MM.
D. MEETS JEDEC.95 MS-026, VARIATION = BBC. REFER TO THIS SPECIFICATION FOR FURTHER DETAILS.